Phosphide-Based Optical Emitters for Monolithic Integration with GaAs MESFETs

by

Joseph F. Ahadian

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University of California, San Diego (1993)

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Author _____
Joseph F. Ahadian
9 June 1995

Certified by _____
Clifton G. Fonstad, Jr.
Professor of Electrical Engineering
Thesis Supervisor

Certified by _____
Leslie A. Kolodziejski
Associate Professor of Electrical Engineering
Thesis Supervisor

Accepted by _____
Frederic R. Morgenthaler
Chair, Department Committee on Graduate Students
Department of Electrical Engineering and Computer Science

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Abstract

Motivated by the need to overcome several inherent electrical interconnect performance limitations, a recent research thrust aimed at developing an optoelectronic very large scale integration (OE-VLSI) platform has yielded the "Epi-on-Electronics" (EoE) monolithic integration technology. This technology allows the integration of III-V heterostructures and commercial GaAs very large scale integrated (VLSI) metal-semiconductor field effect transistor (MESFET) circuits. These VLSI chips, commercially manufactured by Vitesse Semiconductor Co., have been found to withstand extended temperature cycles of up to approximately 470°C for up to 5 hours without significant degradation of the electronic performance. This time/temperature range is similar to that encountered during the growth of III-V heterostructure light emitting diodes (LEDs) and laser diodes by molecular beam epitaxy (MBE).

A substrate temperature of less than 600°C is not optimal for the conventional growth of AlGaAs-containing LEDs and lasers. However, high performance lasers utilizing InGaP ($In_{0.49}Ga_{0.51}P$ is lattice matched to GaAs) as the wide bandgap material have been realized by a number of groups. Since phosphorus-containing III-V compound semiconductors are nominally grown by gas source MBE below 500°C, optical devices based on this material system are ideal candidates for EoE optoelectronic integrated circuits (OEICs). This thesis investigates EoE compatible, high quality LEDs and lasers based on the InGaAsP material system.

Strained InGaAs/GaAs/InGaP quantum well separate confinement heterostructure lasers having pulsed room temperature broad-area threshold current densities of 200 A/cm^2 have been fabricated. Characterization of GaAs/InGaP LED material heterostructures shows substantial improvement in efficiency over similar GaAs/AlGaAs heterostructures. The aforementioned structures were grown at a constant substrate temperature of 470°C on bulk GaAs.

This thesis also addresses two EoE technology challenges. A robust procedure has been developed for the preparation of dielectric growth windows (DGWs) on integrated circuits intended for growth. Also, the normal MBE practice of briefly elevating the substrate temperature to 580°C to desorb the native GaAs oxide prior to MBE growth results in damage to upper-level metal interconnects. Preliminary investigation of a low temperature native oxide removal technique utilizing hydrogen plasma is reported.

The results of this thesis--reliable DGW preparation, low temperature native GaAs oxide removal, and EoE compatible growth of high quality LEDs and laser diodes--represent a significant refinement of the EoE integration technique for the fabrication of high performance OEICs.

Thesis Supervisor: Clifton G. Fonstad, Jr.
Title: Professor of Electrical Engineering

Thesis Supervisor: Leslie A. Kolodziejski
Title: Associate Professor of Electrical Engineering

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With complete sincerity and for reasons too numerous to list, I thank God.

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Chapter 1

Introduction

1.1 Motivation for Optical Interconnects

Great advances in the scaling of electronic devices have brought integrated circuit technology to the point where electrical interconnect throughput is the primary limitation to overall system performance rather that transistor switching speed [1,2]. As clock frequency, the primarily gauge of processing speed, reaches the 100 MHz to 1 GHz range, circuit parasitics and distributed wave phenomenon must be addressed. The design costs associated with overcoming the limitations of electrical interconnects are measured in terms of engineering resources and time-to-market. In a competitive technology market, these growing costs are intolerable. While sophisticated design methodology can continue to push conventional interconnect technology to meet incrementally higher performance requirements in the foreseeable future, it is likely that substantial performance improvements will not be possible without directly addressing the interconnect bottleneck. Optical interconnect technology, used in conjunction with conventional electronics, is a solution to these technological and economic problems.

A number of the important limitations of conventional inter- and intra-chip electrical interconnects can be identified.

- Electromigration: Careful design of multilevel metallization is required to control electromigration-induced failure of metal interconnects in current VLSI technology [3]. This failure mechanism will be even more pronounced at the higher current densities needed to increase clock speed. It is uncertain if process advancements will allow this increase in clock speed [4].

- Distributed circuit effects: As switching speeds increase, finite wave propagation effects must be accounted for in interconnect design; interconnects must be treated as transmission lines and must be appropriately terminated. Such impedance matching not only increases interconnect complexity, but results in an appreciable

power increase.

• Signal skew: At high frequencies, the propagation delay from point to point is influenced by the parasitic capacitances of structures adjacent to the line, so control of signal skew, as in clock distribution, becomes a major effort [4].

• Crosstalk: Capacitive coupling of finely spaced lines increases with frequency, resulting in significant crosstalk between them [4].

• Electromagnetic interference: If an application involves both microwave and high speed digital circuitry, as in portable communication applications, reception and radiation of electromagnetic interference by the interconnect lines becomes a problem. Assuming adequate electromagnetic isolation is practical, a tremendous effort is still required to design it.

• Massively parallel connectivity: In applications where massively parallel interconnects are required, such as supercomputer or neural network architectures, electrical interconnects are impractical due to the rigid restrictions that must be placed on wire routing in order to retain manufacturability. Optical signals, on the other hand, can be intersected or transmitted through free space.

Optical interconnect technology provides solutions to these problems.

1.2 Optoelectronic Very Large Scale Integration (OE-VLSI)

The components in an optical interconnect system include optical emitters, detectors, light propagation media, and modulators. The emitter may be a light emitting diode (LED) or laser diode. Possible photodetectors include the metal-semiconductor-metal photodetector (MSM), PIN photodetector, optical field effect transistor (OPFET), and others. The optical signals may propagate in free space or through a waveguide structure, such as an optical fiber or planar waveguide. Modulation of optical signals may be desired surface-normal or in-plane. In all cases, optoelectronic devices must be tightly coupled to very high density electronics. How these components may best be used in an actual application is a question that will only be answered by the demonstration of real optoelectronic integrated circuits (OEICs). An OEIC platform that is flexible enough to include many types of architectures, sophisticated enough to allow the advantages of optical interconnects to be measured, and

practical enough to be realized in the short term must be developed.

The combination of large numbers of optoelectronic devices with high density electronics is termed OE-VLSI (OptoElectronic-Very Large Scale Integration). There are two distinct approaches to integration: hybrid and monolithic. Hybrid integration combines discrete optoelectronic devices with VLSI components on a multi-chip module. The inability to intermix a large number of such optical devices with the electronics, and the increased capacitance and inductance of off-chip routing of electrical signals, results in density, power, and speed limitations. This renders hybrid integration a short term solution for many applications.

In monolithic integration, both electronics and optoelectronics are contained on the same substrate. This may be accomplished by using an epitaxial lift-off technique wherein electronics and optoelectronics are fabricated on separate substrates which are then fused. However, manufacturing difficulties limit the yield of high density/high area systems.

A fully integrated and monolithic approach is to grow the necessary epitaxial layers for both the optoelectronics and the electronics on the same substrate and then process individual devices from the appropriate layers. Implementation of this technique, however, would require the development of many new fabrication processes to address uniformity and manufacturing issues.

An "electronics-first" approach, where chips based on a mature electronics technology are used as substrates on which optoelectronic devices are grown, provides a fully monolithic integrated solution that can be implemented with minimal new process development. By adding optoelectronics to a mature electronics technology, the integration process is reduced to that of conventional optoelectronic device fabrication.

On what electronics technology should electronics-first OE-VLSI be built? A desirable choice is silicon complementary metal-oxide-semiconductor (CMOS) technology

due to its low cost and great accessibility. However, numerous attempts to grow compound semiconductors on silicon substrates have met with little success due to the large mismatch in lattice constant and thermal expansion coefficient. Compound semiconductor substrates are required for compatibility with III-V optical devices. GaAs or InP heterojunction bipolar transistor (HBT) electronics require complicated fabrication processes and large device sizes that are not suitable for scaling to next-generation integration levels. VLSI level circuits based on GaAs metal-semiconductor field effect transistor (MESFET) technology are commercially available from Vitesse Semiconductor, Inc., and Motorola, Inc. Utilizing fabrication processes very similar to silicon CMOS, this technology will scale to ultra large scale integration (ULSI) levels.

1.3 Epi-On-Electronics (EoE)

An OE-VLSI technology based on the electronics-first approach using GaAs MESFET electronics has been demonstrated [5,6,7,8,9]; it is referred to as Epi-on-Electronics (EoE). In this technique, the electronic portion of the OEIC is designed using standard computer aided design (CAD) tools and submitted to MOSIS, a government sponsored microfabrication service. The design includes the specifications for dielectric growth windows (DGWs) which expose the underlying GaAs substrate to provide seed crystal for growth. Under contract to MOSIS, Vitesse Semiconductor, Inc., fabricates the chips. Figure 1.1 shows the major steps in the process following receipt of the chips from MOSIS. After an epitaxy window preparation step, the chips are loaded into a molecular beam epitaxy (MBE) reactor for growth. This leaves single crystal material in the windows and polycrystalline material over the rest of the chip. To re-planarize the chip following growth, the epitaxial device material is photolithographically masked and the polycrystalline material chemically etched. After stripping the mask, the material in the DGWs may

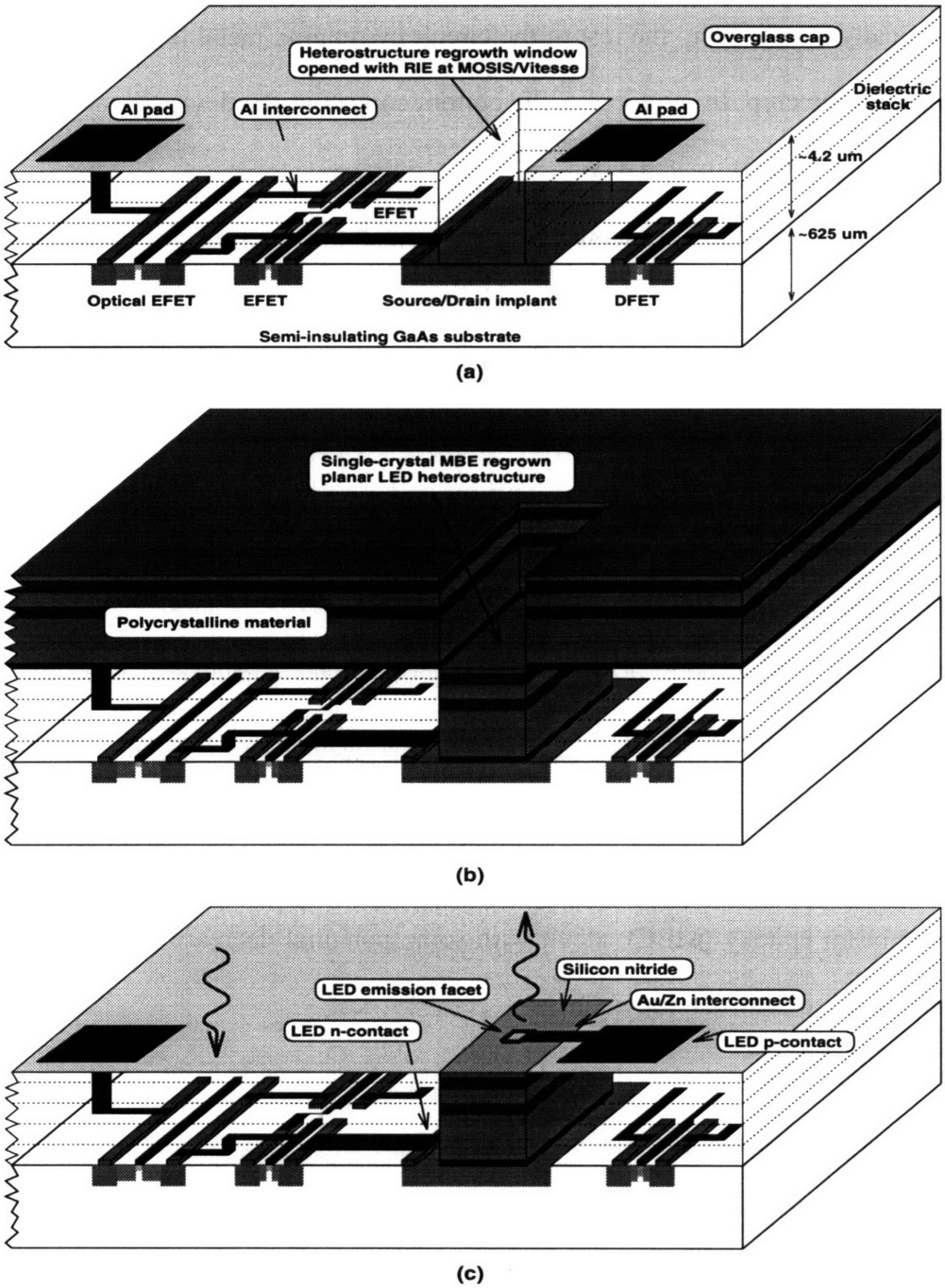


Figure 1.1: Major steps in the Epi-on-Electronics process. (a) Chips are returned from Vitesse with foundry opened epitaxy windows to the GaAs substrate. (b) Following growth, single crystal material is found in the windows while the rest of the chip is covered with polycrystalline deposits. (c) The polycrystalline material is etched off and optoelectronic devices are fabricated. These devices are connected to the electronics by running metal lines to bond pads on the surface.

be processed into optoelectronic devices using standard techniques. Finally, the devices are electrically connected to the rest of the circuit by running metal lines to bond pads on the surface of the chip. In most cases, the bottom contact to the device is made through a standard n-type implant in the DGW.

Any kind of compound semiconductor device that is lattice-matched to GaAs may be integrated with high density MESFET electronics using this method. In addition to enhancement-mode and depletion-mode MESFETs, the standard Vitesse process can be used to fabricate MSM and OP-FET photodetectors. Using the EoE technique, working prototype OEICs have been demonstrated [9].

1.4 Thesis Overview

EoE is the starting point of the present work. As reviewed in Chapter 2, thermal stability studies on integrated circuits (ICs) from Vitesse have shown that the transistors and metallization can withstand a time-temperature cycle of 5 hours at 470°C without degradation. This makes it possible to grow optoelectronic device material using the technique of molecular beam epitaxy (MBE), albeit with some potential decrease in material quality due to the reduced growth temperature

Established LEDs and laser diodes use $Al_xGa_{1-x}As$ as a wide bandgap cladding layer. Aluminum-containing compounds, however, are optimally grown, by conventional MBE techniques, at around 700°C [10]. Emitter performance will be compromised if they are grown in a manner compatible with EoE integration, unless more sophisticated growth methods, such as migration enhanced epitaxy or stoichiometric growth, are used [11,12,13,14,15,16]. To avoid growth complication, thus increasing the practicality and manufacturability of the integration procedure, this thesis seeks to develop LEDs and lasers that can be grown within the allowed EoE thermal budget by using InGaP

($In_{0.49}Ga_{0.51}P$ is lattice-matched to GaAs) as the wide bandgap material in place of AlGaAs. The $In_xGa_{1-x}As_yP_{1-y}$ material system is nominally grown below 500°C, therefore phosphide-based emitters grown under EoE compatible conditions should perform optimally. This motivation is elaborated in Chapter 2.

In addition to developing efficient emitters, this thesis addresses EoE integration issues. The epitaxy window preparation procedure developed in the initial EoE studies was used in the early phases of this work. Problems with and modifications to this procedure are described in Chapter 3.

The use of InGaP allows the bulk of the MBE growth cycle to be carried out below 500°C. However, the normal MBE practice of thermally desorbing the native GaAs oxide requires a brief excursion to above 580°C. This temperature exposure is enough to substantially degrade the upper-level metals of the ICs. In Chapter 4, a technique using atomic hydrogen to remove the oxide is described. This process removes the oxide well below 500°C, and enables the entire MBE growth process to be carried out without damage to the electronics.

The material quality of InGaP, GaAs, and InGaAs, grown at 470°C, is qualified in Chapter 5. For very low power/high density applications, LEDs are an attractive light source because no threshold power is required for operation. Chapter 6 presents the development of LEDs based on the GaAs/InGaP double heterostructure. For applications requiring higher power and/or speed, laser diodes are more effective. Chapter 7 demonstrated a strained InGaAs/GaAs/InGaP quantum well separate confinement heterostructure (QW-SCH) laser diode.

The combined results of this thesis, namely reliable DGW preparation, low temperature GaAs native oxide removal, and EoE compatible growth of high performance optical emitters, greatly extend the functionality of EoE integration.

Chapter 2

Epi-on-Electronics OE-VLSI and Phosphides

2.1 Thermal Stability of GaAs MESFET ICs

The primary constraint on material growth for EoE integration is the limited thermal stability of the electronics. As with silicon CMOS, the achievement of VLSI level integration in GaAs MESFET technology depends on the self-alignment of source and drain implants to the gate. This means that the gate material must be able to withstand the high temperature anneal (800°C for one hour in the case of the Vitesse process) that is required to activate the implant. In CMOS, this is accomplished, by using polycrystalline silicon for the gate. In commercial MESFET processing, high temperature stability of the Schottky gate is attained from refractory metal based contact, such as $W_{1-x}N_x$. The fact that the gate can withstand an extended exposure to such high temperatures inspired investigation into the thermal stability of completed ICs [7]. These studies established the possibility of MBE growth in foundry opened epitaxy windows on fully processed chips.

2.1.1 Thermal Stability Results

Investigation of the thermal stability of Vitesse GaAs MESFET VLSI ICs by Braun, *et al.*, has led to an understanding of the degradation mechanisms and illuminated the boundaries of the time/temperature "growth envelope" [17,18]. Thermal cycles were performed on electrical test structures located on Vitesse HGaAs3 process control monitors. As summarized in Appendix D, the Vitesse process includes Schottky contacts for MEFSET gates, ohmic contacts to the source/drain regions, and "upper level" (metal 1 through metal 3 on the chips tested) metal interconnects. The Schottky gate contact itself was found to be stable for all thermal cycles [17], as originally expected. However, the upper

level metal sheet resistances and ohmic contact resistances were found to degrade as the result of thermally activated metallurgical reactions [18].

Five hour thermal cycles, corresponding to the growth time for integrated structures, were carried out at various temperatures. Figure 2.1 shows the gate, ohmic, and interconnect metal sheet resistances as a function of anneal temperature. The gate and ohmic metal

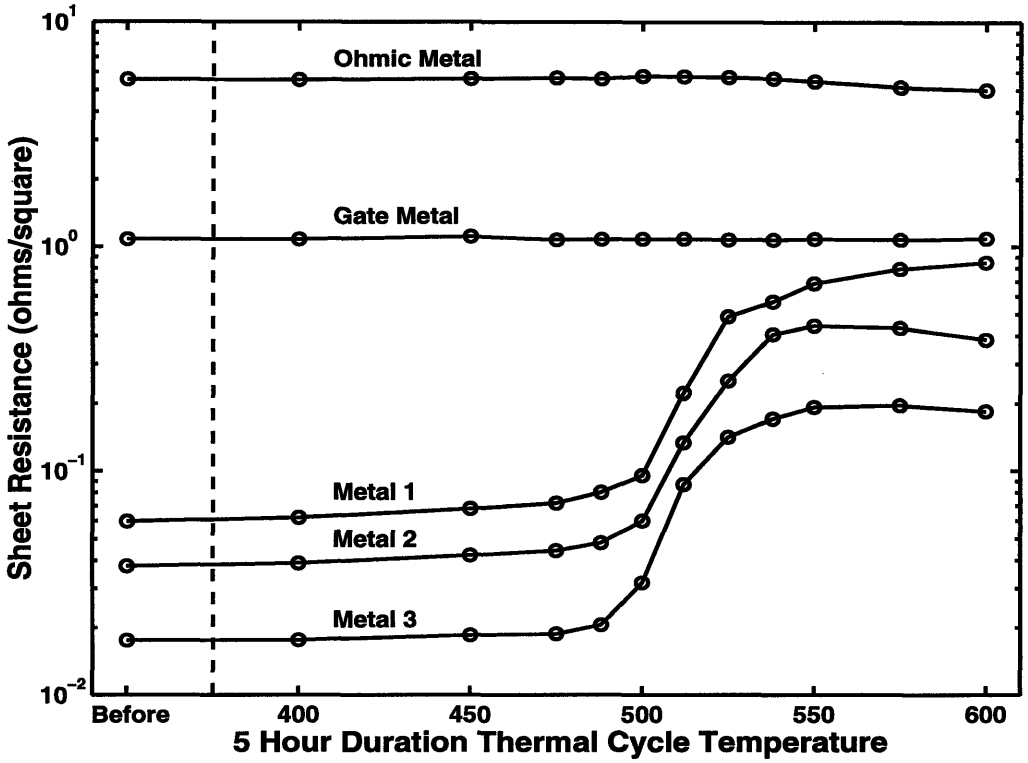


Figure 2.1: Interconnect sheet resistance after 5 hour thermal cycles [18]

layers displayed almost no sheet resistance change even after 5 hours at 600°C. However, between 400°C and 600°C, the aluminum-based metal 1 through 3 layers increased significantly in sheet resistance. This resistance increase is believed to be the result of a metallurgical reaction between the $AlCu_x$ core and WN_x cladding. Increasing the nitrogen content in the WN_x layers produced interconnects that did not exhibit an increase in sheet resistance when annealed below 550°C for five hours [18].

The metal 1 sheet resistance increased linearly in time, the underlying reaction being thermally activated. The sheet resistance increase saturated at approximately 15 times the non-annealed value. Using an Arrhenius based model, a set of theoretical curves was fitted to the measurements of metal 1 sheet resistance for arbitrary times in the temperature range of 400°C to 600°C. Figure 2.2 shows this model with excellent agreement to experimental results [18].

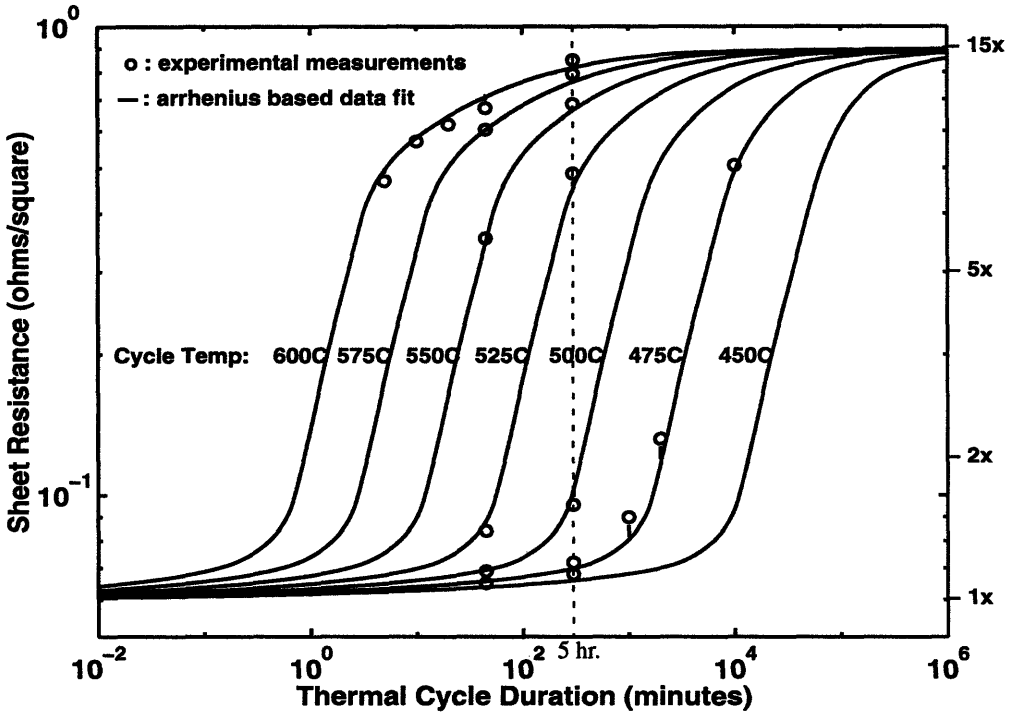


Figure 2.2: Theoretical and measured metal 1 sheet resistance thermal cycle responce. The Arrhenius based model indicates an activation energy of 3.5 eV [18].

The ohmic contact resistance increase was also thermally activated and progressed linearly in time, but the onset of the resistance increase was delayed in time. This delay was found to depend strongly on the distance between the metal 1 via edge and the ohmic contact metal edge. Figure 2.3 shows the average measured MESFET source resistance and small and large transmission line model (TLM) resistances per unit contact length as a function of anneal temperature. (In the figure, "critical temperature" is defined as the tem-

perature where the resistance per unit contact length exceeded 2000 ohm-μm.) A reaction

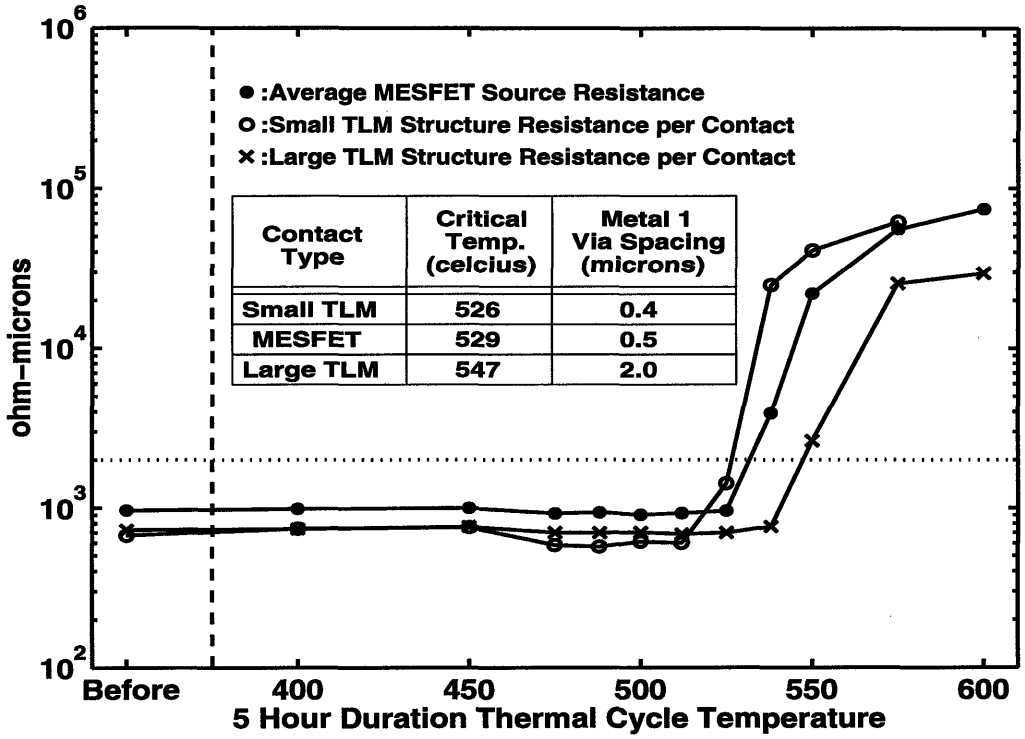


Figure 2.3: Ohmic contact resistance after 5 hour thermal cycles for MESFET sources and large and small TLM structures. The inset gives the 2000 Ω–μm critical temperature and metal 1 via spacing for each ohmic contact structure. [18]

between the Al-Cu-W-N interconnect and Ni-Ge contact is the cause of the ohmic contact resistance increase. The time delay is associated with the diffusion of the aluminum compound to the ohmic contact metal edge through the WN_x barrier. The barrier consists of the metal 1 bottom cladding layer, the ohmic metal top layer, and the via top spacing layer, which explains the correlation between the ohmic contact to metal 1 via spacing and the delay of the onset of the resistance increase [18].

As with the interconnect metal sheet resistance, the strong temperature dependence of the ohmic contact resistance can be modeled as a thermally activated process. Figure 2.4

gives a set of curves suitable for approximating this resistance for arbitrary thermal cycle temperatures and durations.

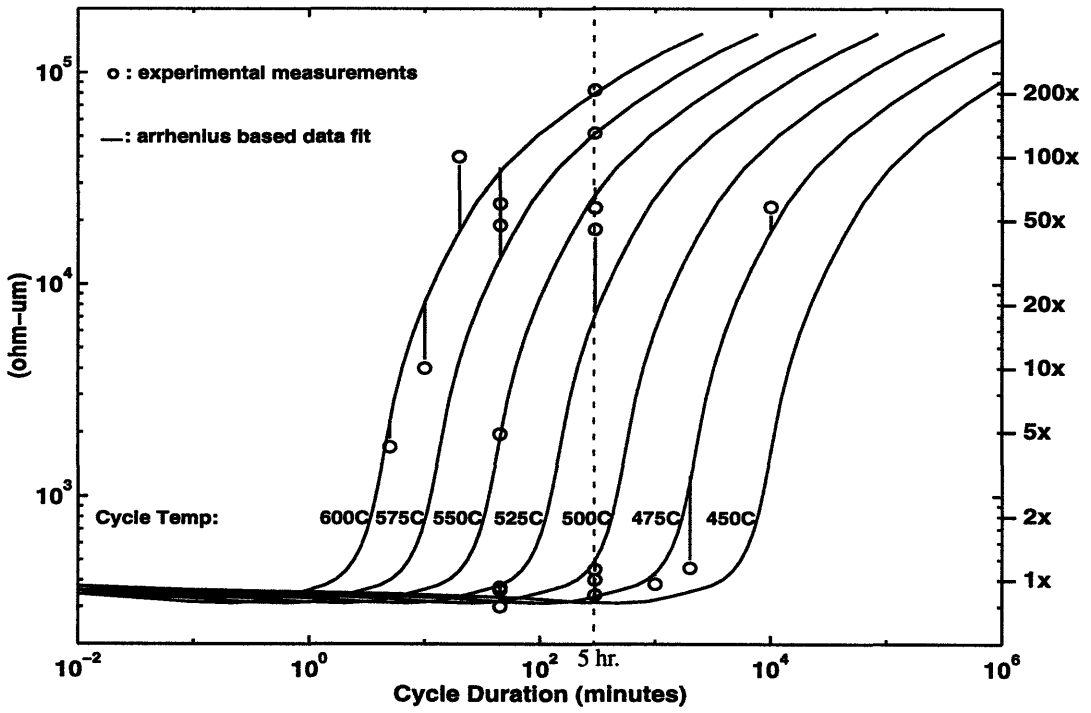


Figure 2.4: Theoretical and measured metal 1-ohmic metal-implant contact resistance thermal cycle response. The Arrhenius based model indicates an activation energy of 2.5 eV to 2.8 eV [17]

Finally, to test the effect of the thermal cycles on actual circuit performance, 23-stage direct-coupled field effect transistor logic (DCFL) ring oscillators were also tested. Oscillation frequency was unchanged for anneals up to 450°C. Between 450°C and 540°C, the ring oscillator period increased by 10%. No oscillations were observed for anneals at or above 550°C. Using the measured ohmic contact resistances, HSPICE simulations of the ring oscillator correctly predicted that the circuit would not oscillate after a 540°C anneal [18].

2.1.2 Thermal Budget

The importance of the thermal stability results to the present work is in establishing safe time/temperature exposure limits for Vitesse ICs used in EoE MBE growth. Figure 2.2 and Figure 2.4 indicate that a thermal cycle of 5 hours at 470°C will not compromise electronic circuit performance. This temperature also allows for a reasonable tolerance in setting the substrate temperature during growth, and is nearly optimal for the growth of InGaP. The growth temperature of 470°C was thus chosen for the structures investigated in Chapter 6 and Chapter 7. It is also important to note that even a brief exposure to temperatures near 600°C causes significant degradation of the electronics. This motivates the work on low temperature oxide removal presented in Chapter 4.

2.2 AlGaAs-Based Laser Diodes

Since $Al_xGa_{1-x}As$ is essentially lattice-matched to GaAs for all mole fractions, and exhibits a direct bandgap for aluminium concentrations below approximately 40%, it is the most mature III-V material system investigated. High quality semiconductor laser diodes using AlGaAs/GaAs have long been fabricated. Such a device was the target of initial EoE integration efforts. But, as discussed below, the reduced growth temperature requirements of EoE integration results in compromised performance. InGaP based lasers provide uncompromised electronic and optoelectronic device performance.

The theory and design of in-plane semiconductor laser diodes are explained in Appendix B.

2.2.1 Optimal AlGaAs-Based Laser

A strained InGaAs/GaAs/AlGaAs quantum well graded-index separate confinement heterostructure (QW-GRINSCH), demonstrated by Williams, *et al.*, has one of the lowest reported threshold current densities, 56 A/cm^2, of any semiconductor laser [10]. The

growth structure is diagramed in Figure 2.5. To achieve this result, the authors included

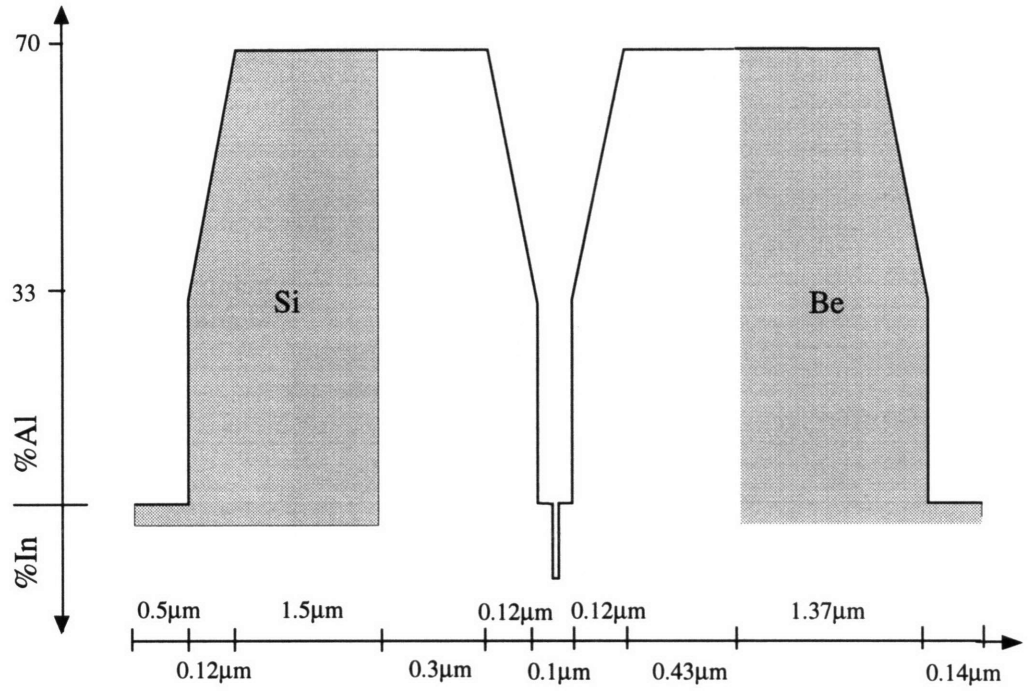


Figure 2.5: Strained InGaAs QW-GRINSCH laser structure used by Williams, *et al.* to attain the low room temperature pulsed broad-area threshold current of 56 A/cm^2. The AlGaAs layers are grown at 700°C while the GaAs and InGaAs are grown at 565°C; the temperature is ramped without growth interruption. The structure is grown on an n-type substrate.

the use of a graded core region for improved current "funneling", graded interfaces to reduce series resistance, set-back of doping to reduce free-carrier optical absorption, and the growth of each layer at the optimal temperature. This meant a substrate temperature of 700°C during growth of the AlGaAs layers.

2.2.2 EoE Optimized AlGaAs Based Laser

It is clear that the optimal growth temperatures used by Williams, *et al.*, are not compatible with EoE integration. In the original work on EoE, Shenoy, *et al.*, optimized a laser structure for low temperature growth [5]. The heterostructure is given in Figure 2.6. The low temperature optimizations include the reduction of aluminium content and the

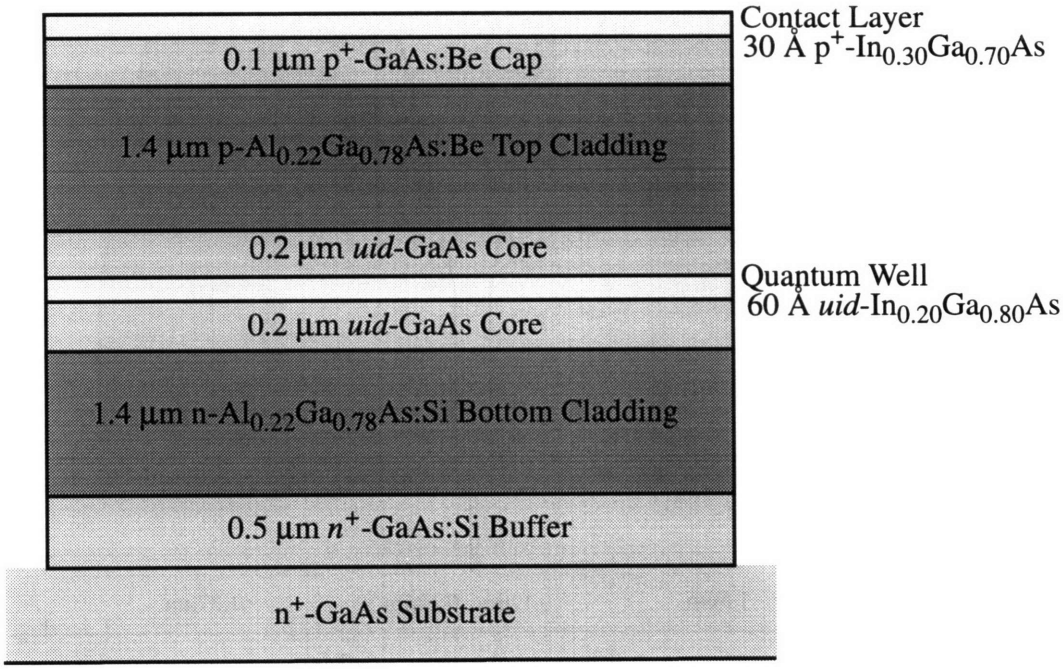


Figure 2.6: Strained InGaAs/GaAs/AlGaAs QW-SCH laser structure used by Shenoy, *et al.*, in original EoE work. This structure is optimized for low temperature growth. The resulting broad area room temperature pulsed threshold current density is 1800 A/cm^2 [5].

increase of the thickness of the unintentionally doped GaAs core layers between the AlGaAs claddings and the quantum well. With these modifications in place, a room temperature pulsed broad-area laser threshold current density of 1800 A/cm^2 was achieved using a growth temperature of 530°C (Increasing the growth temperature to 600°C reduced the threshold current density to 740 A/cm^2, which is higher than necessary since the design was optimized for low temperature growth.). The performance of this low temperature grown laser may be suitable for some applications, but the low power levels needed for high density optoelectronic integration will require more efficient laser diodes.

2.2.3 Unconventional Low Temperature Growth of AlGaAs

Both of the above lasers were made using "conventional" MBE growth techniques. Low temperature growth of AlGaAs based lasers has also been attempted by nonconven-

tional means. For the most part, these methods improve material quality by increasing the surface mobility of Al adatoms. In migration enhanced epitaxy (MEE) the As overpressure is disrupted to allow group III adatoms adequate time to find appropriate lattice sites [11,12,13]. Using this technique, AlGaAs/GaAs broad area laser diodes grown at 350°C were fabricated with room temperature pulsed threshold current densities of 2500 A/cm^2 [14]. While promising, MEE is difficult to implement due to the need for precise, closed-loop control of frequent shutter operations. Another way to enhance adatom mobility is to lower the group V overpressure. Using a III:V flux ratio of nearly unity, AlGaAs based lasers with broad area room temperature pulsed threshold current densities of 600 A/cm^2 have been reported [15,16]. Precise control of As flux is possible in both solid and gas source MBE, but care must be taken to maintain the near stoichiometric growth conditions over varied growth rates, and in spite of run-to-run drift in group III effusion cell fluxes. This technique is promising and requires additional investigation. The ideal growth technique, however, is the simplest one that produces the desired level of performance. Convention growth of aluminum-free materials is a solution.

2.3 AlGaAs and InGaP

The underlying problem with aluminum-containing III-V semiconductors is the presence of aluminum. Difficulties with aluminum-containing compounds arise both during and after growth. Aluminum has a very high affinity for oxygen, making it difficult to prepare oxygen-free samples [19]. Once incorporated in AlGaAs, the oxygen acts as an efficient nonradiative recombination center [20,21].

Nonradiative recombination increases the threshold current of a laser by diverting carriers from the quantum well and generating heat. In a PiN laser diode, the presence of nonradiative recombination centers in the bulk P and N regions (that is, the cladding layers) is

relatively unimportant compared to the undoped core and active region (quantum well(s)). Since recombination centers act to return a system to thermal equilibrium, they are not of great consequence in the highly doped claddings where the excess carriers present only a small deviation from equilibrium. In the undoped regions, however, the presence of excess minority carriers represents a large perturbation, making the injected carriers very vulnerable to recombination centers. Since oxygen incorporation in the undoped GaAs core or InGaAs quantum well is not significant, it is the presence of nonradiative recombination centers at the AlGaAs/GaAs interface that most likely limits AlGaAs laser performance. It has, in fact, been found that interface nonradiative recombination processes are responsible for high threshold currents [22].

Carrier recombination at an interface is characterized by the interface recombination velocity, which is adversely effected by the incorporation of oxygen in aluminium containing compounds [23]. Table 2.1 gives the interface recombination velocities for InGaP, AlGaAs, and InAlP; both cases involving aluminum are significantly greater that the aluminum free InGaP.

$Al_{0.4}Ga_{0.6}As/GaAs$	210 cm/s
$In_{0.5}Al_{0.5}P/GaAs$	900 cm/s
$In_{0.5}Ga_{0.5}P/GaAs$	1.5 cm/s

Table 2.1: Upper bound on interface recombination velocity [23].

It has been found that below 700°C, the incorporation of oxygen in AlGaAs is arrival rate limited with unity sticking coefficient, and that oxygen accumulates at AlGaAs/GaAs interfaces. This is consistent with a model in which oxygen adsorbs to the growth surface by forming an aluminum oxide [24]. At higher temperatures the oxygen and aluminum are less tightly bound and the oxygen is able to desorb, possibly aided by gallium desorption

[25]. Thus, oxygen incorporation is increased at lower growth temperatures, explaining the higher threshold current of the low growth temperature InGaAs/GaAs/AlGaAs lasers of Shenoy, *et al.* [5].

Even after the growth and processing of AlGaAs based lasers, the high oxygen affinity of aluminum continues to be a problem. Oxidation of the laser facets is responsible for catastrophic optical damage (COD), as outlined in Figure 2.7. The nonradiative recombi-

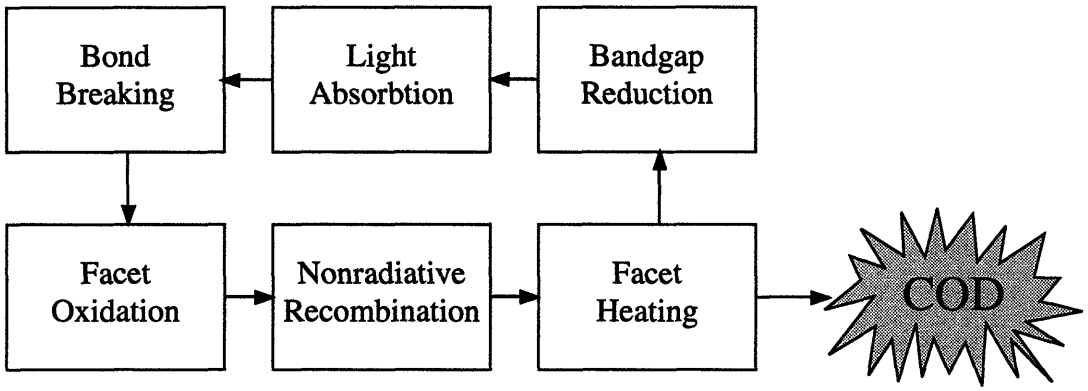


Figure 2.7: Catastrophic optical damage is a consequence of facet oxidation. Incorporated oxygen results in nonradiative recombination which produces local heating of the facet. A positive feedback loop is formed when the rise in temperature causes bandgap reduction. This increases the light absorbtion near the facet, which increases the aluminium oxidation reaction by breaking aluminium bonds [26].

nation resulting from oxygen incorporated into the material near the facet results in a temperature rise. The oxidation process is aided by bond breaking caused by light absorbtion. Since light absorbtion is increased when the bandgap is reduced due to the temperature rise, a positive feedback loop occurs [26]. For optical power levels above the "COD threshold" this system becomes unstable and rapidly destroys the laser facet. COD brings into question the reliability of AlGaAs lasers. As detailed in Section 2.4, this reliability question led to work on aluminium free lasers.

2.4 Phosphide-based Laser Diodes

Ijichi was the first to suggest the use of InGaP in place of AlGaAs in the basic InGaAs/GaAs quantum well laser structure [27]. The motivation for this work was the pumping of Er^{3+} doped fiber amplifiers (EDFA), which are a critical component in long haul optical communication systems. An EDFA may be pumped at either 0.98 μm or 1.48 μm, but when pumped at 0.98 μm the Er^{3+} atoms behave as an ideal three level system, yielding higher pumping efficiency. Long term reliability and high output power over a wide range of operating temperatures are required for EDFA pump lasers [26,28,29]. InGaAs/GaAs/AlGaAs lasers have historically filled this role [30], but catastrophic optical damage (COD) limits the reliability of these devices [26,31]. Studies of facet temperature and COD in aluminium-free lasers have provided evidence that the removal of aluminium improves laser reliability [26,32,33,34].

Aside from the reduced facet oxidation, the presence of donor related deep traps (DX centers) in AlGaAs:Si makes it difficult to achieve high carrier concentrations [35], while InGaP shows no significant DX center concentration [36]. Furthermore, the use of InGaP simplifies the fabrication of buried heterostructure lasers since little surface oxide is formed between growth steps. Also, the fabrication of InGaP/GaAs based devices is aided by the availability of selective wet and dry etches [37]. Most importantly for EoE applications, the low InGaP/GaAs interface recombination velocity results in a reduced threshold current in InGaP lasers compared to the AlGaAs counterparts, particularly those grown at EoE compatible temperatures.

This section reviews the development of InGaP based high power laser diodes for EDFA pumping applications. This provides a useful introduction to the various device structures and the issues involved in laser diode design.

2.4.1 Single Quantum Well Separate Confinement Heterostructure (SQW-SCH)

Similar to Ijichi's initial device [27], an aluminium-free laser was fabricated by Pessa, *et al.*, using the single quantum well separate confinement heterostructure (SQW-SCH) in Figure 2.8 [38,39]. Gas source MBE (GSMBE) was used. The InGaP and InGaAs layers

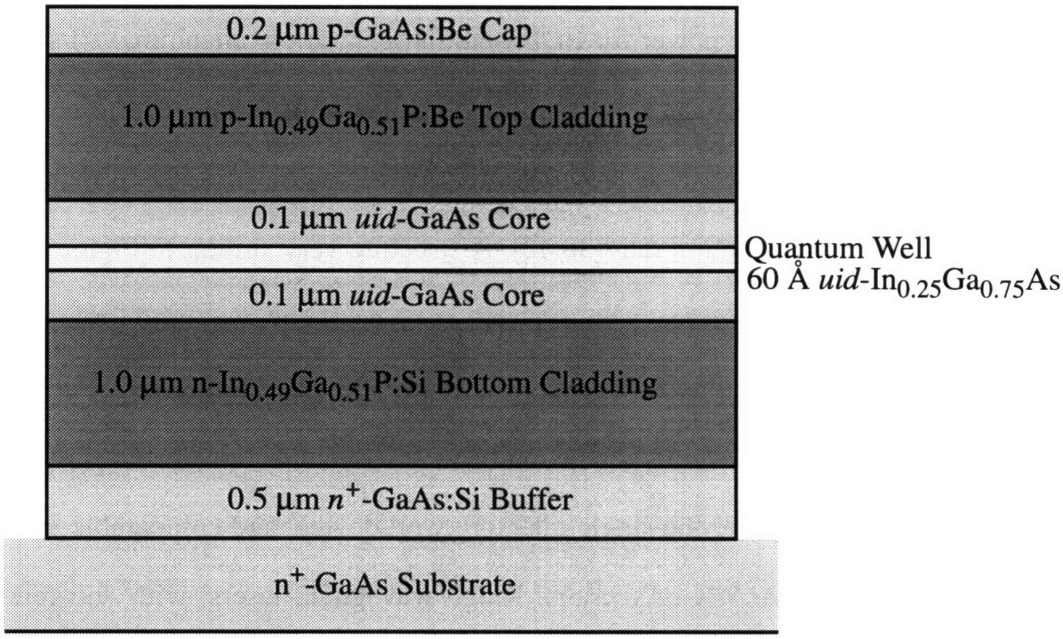


Figure 2.8: InGaAs/GaAs/InGaP QW-SCH used in [38,39]. The GaAs and InGaAs were grown at 590°C and the InGaP at 500°C; after growth, a rapid thermal anneal of 900°C for 1 s was used to improve threshold current. For broad area devices, the pulsed room temperature threshold current was 72 A/cm^2, and the characteristic temperature was approximately 130°K.

were grown at a substrate temperature of 500°C, and the GaAs at 590°C. Before processing, the sample was annealed for 1 s at 900°C using a rapid thermal annealer (RTA) to improve the threshold current by reducing the density of non-radiative recombination centers in the InGaAs quantum well [40]. Broad area lasers had a room temperature pulsed threshold current density of 72 A/cm^2. This compares favorably to the best AlGaAs based lasers. The characteristic temperature T_0, which gives an indication of the temperature sensitivity of the threshold current, was between 120°K and 140°K, in agreement with Iji-

chi's T_0=130°K [27], and T_0=140°K reported for a similar InGaAs/GaAs/AlGaAs laser [41].

2.4.2 Multiple Quantum Well Separate Confinement Heterostructure (MQW-SCH)

Although single quantum well lasers tend to have the lowest threshold current densities, to generate high output power for EDFA pumping, multiple quantum well structures are preferred. As a result of band-filling, more quantum wells are needed to contain the larger charge density that must be present in the active region in order to maintain the higher stimulated recombination rate [38,42]. A structure very similar to Figure 2.8, also grown by GSMBE but using three quantum wells in place of one, was used for high output power lasers [42,43]. The broad area device fabricated exhibited a threshold current density of 177 A/cm^2, or 59 A/cm^2 per quantum well. Its characteristic temperature was 150°K, an improvement over the single quantum well device, and comparable to similar high power InGaAs/GaAs/AlGaAs lasers. Ridge waveguide lasers, with anti-reflection and high reflection facet coatings, were also fabricated. For a 500 μm long, 3 μm wide stripe, having threshold current of 12 mA, the peak output power was 160 mW. The device operated at up to 185°C, and had a characteristic temperature of 180°K

The T_0 of the 3QW InGaAs/GaAs/InGaP lasers was limited by carrier confinement in the quantum wells. The quantum well carrier population is effected by thermionic emission over the barrier, the lifetime of which depends exponentially on $E_{barrier}/k_BT$ [44]. Replacing the GaAs core with a wider bandgap material increases electron confinement, and thus carrier injection efficiency, by raising the quantum well barriers. This has the additional advantage of reducing the optical field confinement, producing a broader mode which will reduce facet heating and astigmatism in the output (the latter is very important to the coupling of light into single mode optical fibers). This approach was used in high

power InGaAs/InGaAsP/InGaP lasers [45,46,47,48,49]. An optimized heterostructure is shown in Figure 2.9 [48,49]. The authors note that using GaAs barriers immediately adja-

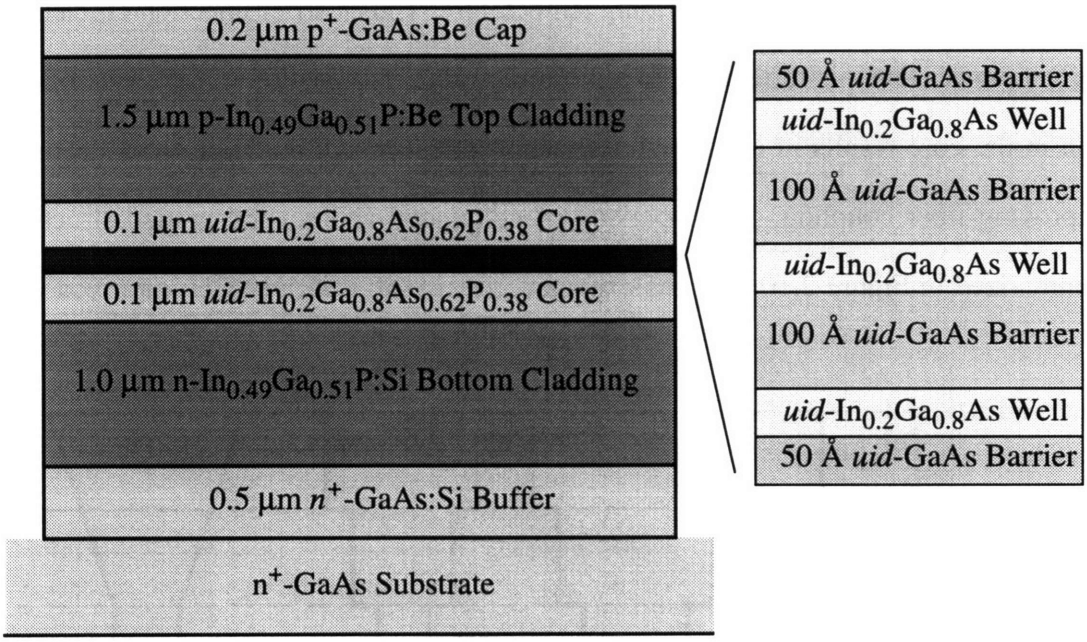


Figure 2.9: Optimized InGaAs/InGaAsP/InGaP high power 3QW-SCH [48,49]. The InGaAsP core layers have E_g=1.57 eV. Using GSMBE, the InGaP and InGaAsP were grown at 500°C by GSMBE; the GaAs at 590°C, and the InGaAs at 515°C. The broad area room temperature pulsed threshold current was 150 A/cm^2. For ridge waveguide devices, the characteristic temperature was around 150°K under pulsed operation.

cent to the quantum wells simplifies the growth while having no measurable effect of performance [49]. The use of the larger bandgap (E_g=1.57 eV) core material was successful in raising T_0 to between 220°K and 280°K.

2.4.3 Graded Index Separate Confinement Heterostructure (GRIN-SCH)

Another approach to increasing T_0 is the use of a graded heterostructures. MOCVD was used to grow graded index separate confinement heterostructure (GRIN-SCH) single quantum well lasers [28,50,51]. The graded core improves carrier injection by "funneling"

current into the quantum well. Graded interfaces also reduce series resistance by eliminating potential spikes resulting from band offsets. The power dissipation, I^2R, is thereby reduced, and along with it the operating temperature. Thus, carrier injection efficiency, for a given power level, is further improved. Furthermore, the grading of the index of refraction in the core results in a less tightly bound optical mode, reducing facet heating and improving fiber coupling. A comparison of nongraded and several graded structures is summarized in Figure 2.10 [51]. As expected, the use of a GRIN-SCH improved T_0, but

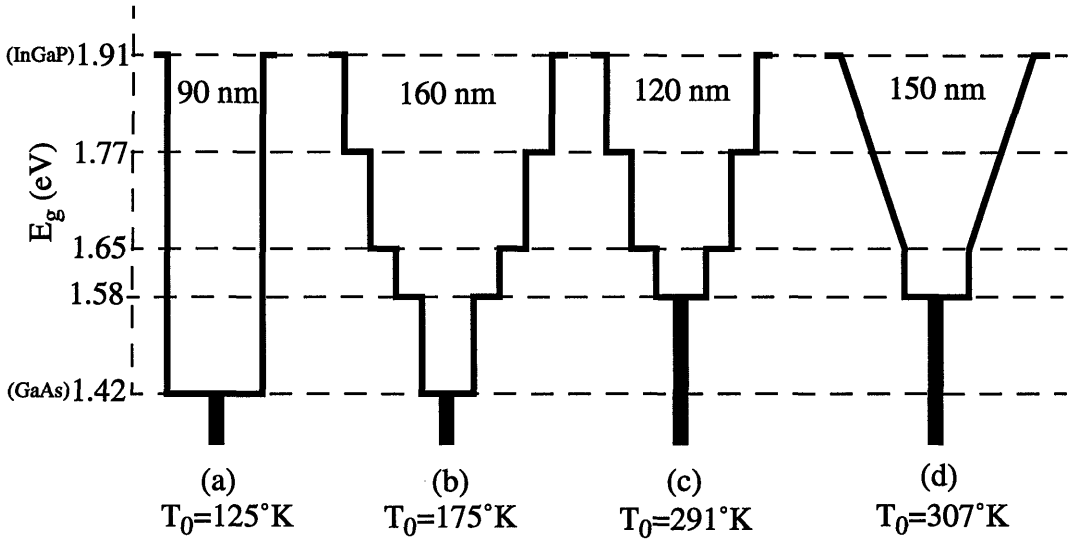


Figure 2.10: Comparison of various SCH cores in terms of the resulting characteristic temperature, T_0, of ridge waveguide lasers [51]. MOCVD was used to grow InGaAsP, lattice matched to GaAs, with the indicated bandgaps. (a) is in agreement with the previously shown QW-SCH result. In (b), T_0 improves due to the current funneling and resistance lowering effects of the grading. The most significant improvement, however, is from simply increasing the quantum barrier, as seen in (c). The small improvement between (c) and (d) indicates that step grading, as in (b) and (c), is adequate to reduce series resistance, and the growth complications associated with continuous composition grading can be avoided. A broad area laser based on (c) had room temperature pulsed threshold current of 220 A/cm^2; this relatively high value is attributed to the low optical confinement of the GRIN-SCH structure [50].

an even more dramatic reduction resulted from increasing the quantum well barrier height. The combined effect produced a characteristic temperature of around 300°K for a ridge

waveguide laser. Also, it was shown that a step grading adequately reduced the series resistance, avoiding the difficult task of maintaining lattice match while continuously varying the InGaAsP composition. The room temperature pulsed broad area threshold current density for structure (c) in the figure was 220 A/cm^2 [50]. This is attributed to the lower overlap of the optical mode with the gain region due to the reduced optical confinement of the GRIN-SCH structure. Since reduced optical confinement aids in coupling light into a single mode fiber, the increase in threshold current may be a justified design compromise in the case of EDFA pumping.

2.5 Device Objectives

This thesis in aimed at the integration of efficient optical emitters with VLSI electronics using the EoE technique. The emitters of interest are LEDs and lasers. Due to the strong tendency of aluminium to oxidize, the AlGaAs based lasers of Section 2.2 can not be optimally grown, in a straightforward fashion, within the thermal budget constraints outlined in Section 2.1. The problems inherent with aluminium containing compounds are avoided by using the InGaAsP material system, and in particular the wide bandgap $In_{0.49}Ga_{0.51}P$ (which is lattice-matched to GaAs). Section 2.4 reviewed work published on InGaP based laser diodes, showing them to be comparable in performance to similar AlGaAs based devices. The growth temperatures reported for these devices are nearly within the EoE thermal budget. It remains to be shown that growth at 470°C can produce good laser and LED performance in the InGaAsP system.

Although much less efficient than lasers, LEDs operate without a threshold. For applications that do not require large optical signals or phase coherence, LEDs are a viable solution. Furthermore, the relative ease of LED fabrication will speed the dissemination of OE-VLSI technology to the systems community, which is critical for the long term devel-

opment of optical interconnect technology. The greatly reduced interface recombination velocity of InGaP is of equal importance in LEDs. Chapter 6 will focus on the fabrication of EoE compatible GaAs/InGaP LEDs.

As discussed in Section 2.4, work on InGaP based lasers has focused on high power devices suitable for pumping EDFAs. For OE-VLSI application, low power dissipation, and thus low laser threshold current, are required. The optimizations made for EDFA pumping are not entirely applicable. For low power use, the most suitable device configuration is the simple SQW-SCH. Chapter 7 develops this device.

Chapter 3

Dielectric Growth Window Preparation

In order to epitaxially grow high quality material in dielectric growth windows (DGWs), a very clean and smooth GaAs surface must be exposed. In the Vitesse standard process, described in Appendix D, a "passivation cut" is normally used to open vias to bonding pads and a "boundary cut" makes trenches though the dielectric stack to allow the wafer to be sawed into chips. The DGWs are defined by specifying, in the circuit layout, passivation and boundary cuts over the regions to be grown.

3.1 Original Preparation Method

Standard photolithographic techniques are used to define the passivation and boundary cut regions. The DGWs are formed using CF_4/O_2 reactive ion etching (RIE) to cut through the roughly 4 μm of dielectric, composed of layers of SiO_2 and Si_3N_4. A by-product of this process is the production of fluorinated hydrocarbons that are redeposited over the surface. SIMS analysis of the residue clearly showed the presence of carbon and fluorine. The fluorinated hydrocarbons act as a mask against further etching. O_2 plasma in the mixture reacts with these organics and partially removes them. However, some organic residue remains in the DGWs after the photoresist is stripped from the rest of the wafer surface. In addition to organic residues, fragments of dielectric are deposited in the DGWs. Thus, a cut reaching down to the GaAs surface is produced, but the surface is covered with a mixture of dielectric and organic residues, as diagrammed in Figure 3.1. Nomarski micrographs of DGWs showing this residue are in Figure 3.2.

In original EoE work, this residue was removed using a combination of CF_4/O_2 RIE and wet etching in buffered hydrofluoric acid (BOE). A typical implementation used 45

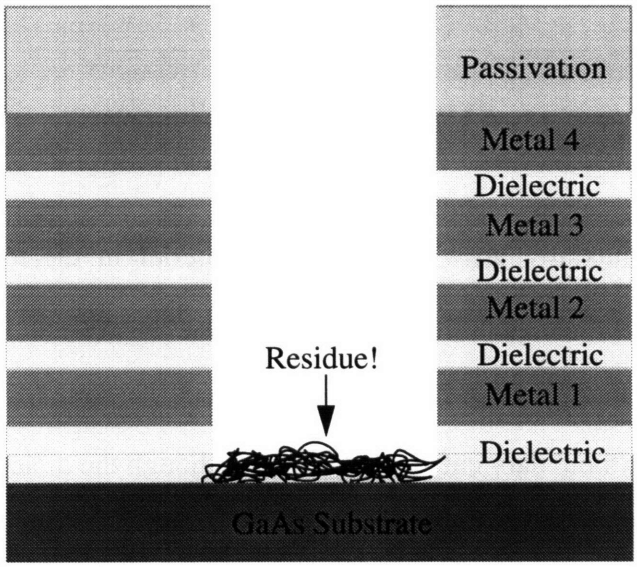


Figure 3.1: Dielectric Growth Window (DGW) cut in dielectric/ metallization stack with CF_4/O_2 RIE. The GaAs at the bottom of the DGW is covered with a mixture of fluorinated hydrocarbons and dielectric fragments produced by the etch.

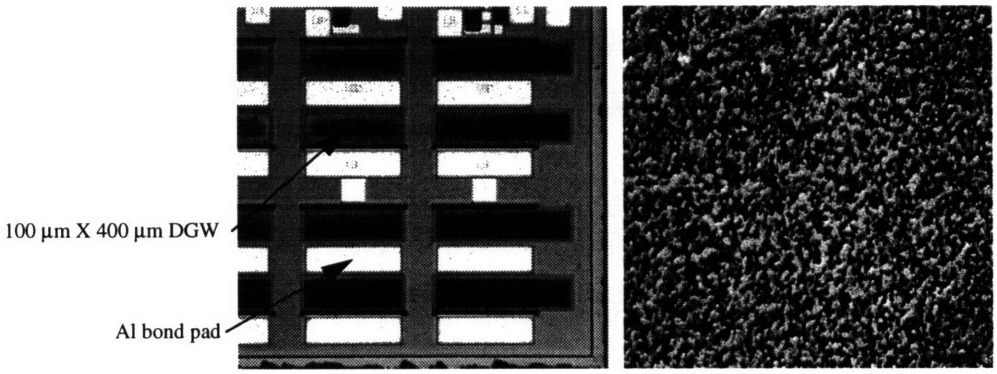
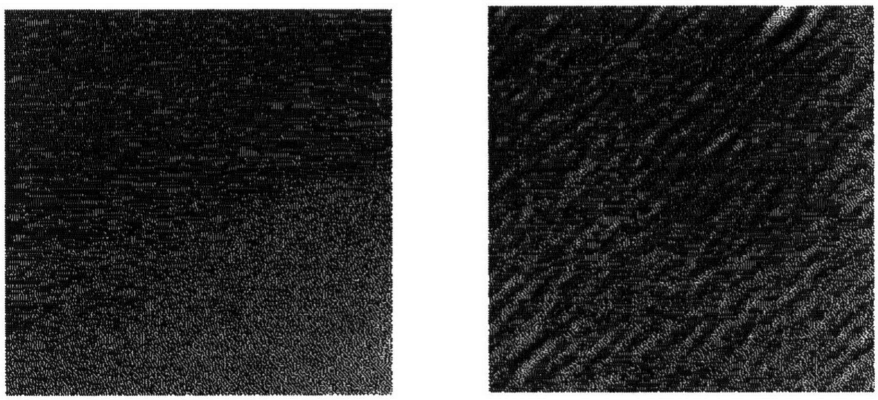


Figure 3.2: Nomarski micrographs of DGWs (a) 50X, note nonuniformity of residue between different DGWs (b) 1000X

sccm CF_4/10 sccm O_2 at 5 mTorr and 200 W incident power for 10 min. followed by a 5 min. dip in BOE (circuit side down) with ultrasonic agitation. BOE etches dielectric, including SiO_2 and Si_3N_4, but etches GaAs only very slowly. This resulted in a visually clean surface with no noticible morphology. The Al bond pads are attacked by the BOE,

but a 5 min. application leaves them in a usable state (longer times produce significant damage). After degreasing with trichloroethane, acetone, and methanol, and an additional 5 second dip in BOE, chips were In mounted alongside a bulk GaAs substrate and put through a standard growth sequence. Figure 3.3 compares the surface morphology of the



(a) (b)

Figure 3.3: 1000X Nomarski micrographs of AlGaAs based LED material (a) on bulk GaAs wafer and (b) in a DGW. The DGW was prepared using a gentle CF_4/O_2 RIE followed by wet etching in BOE. The material in (a) is very smooth. Slight roughness is seen in (b), but this did not effect LED performance.

epitaxial material on the bulk wafer and in a DGW. The material grown on bulk GaAs is featureless. The DGW material is nearly as good, though some striated morphology is visible. LEDs fabricated on this material performed comparably to those fabricated from the material grown on the bulk wafer.

Approximately one year after the AlGaAs LED work, the cleaning method described above was again employed to prepare chips for InGaP LED growths. However, bits of the black residue remained in the DGWs. The failure of the DGW preparation procedure prompted a more through investigation of the residue.

As a first attempt, a chip was placed in an ozone ambient. Ozone, a highly reactive form of oxygen, is often used in microelectronic processing to remove organics. Exposure to ozone had a marked effect, greatly reducing the concentration of black residue, but the rate of residue elimination diminished with exposure, and the residue was not completely removed after an hour in ozone. A more reactive form of oxygen is O_2 plasma. The same chip was cleaned with O_2 plasma in a RIE chamber (90 sccm, 40 mTorr 40 V_{bias}, ~30 W, 40°C). After three hours in O_2 plasma, some of the DGWs were free of the black residue while others seemed untouched, as seen in Figure 3.4. Evidently, the residue deposition is

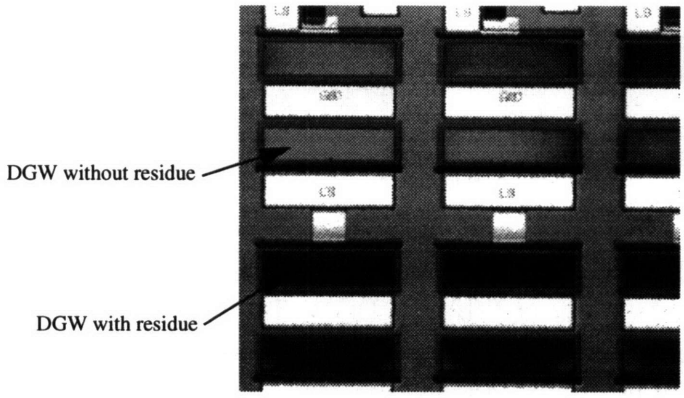


Figure 3.4: 50X Nomarski micrographs of DGWs after 1 hour in ozone and 3 hours in O_2 plasma. Some DGWs are free of black residue (but display surface morphology) while others are heavily coated with black residue.

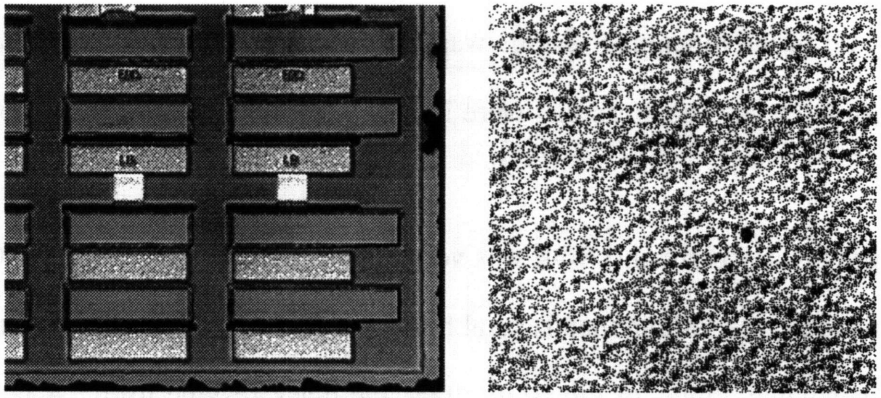
quite nonuniform across the chip. Further exposure to O_2 plasma, up to a total of 5 hours, had no additional effect. Apparently, there is some nonuniform masking of the black residue, presumably the fluorinated hydrocarbon, by the dielectric fragments. It is unclear whether the DGWs that have no black residue are also devoid of dielectric residue, since this material may be transparent. These DGWs did exhibit a great deal of surface roughness.

Following cleaning in ozone and O_2 plasma, the same chip was dipped in BOE. In 1 min. nearly all of the remaining residue was removed. In less than 4 min, all of the wells were uniformly clean, The areas that were free of black residue after the O_2 plasma were unchanged.

In the previous experiment, BOE was very effective in cleaning out the DGW; only 1 minute removed more residue than several hours in O_2 plasma. Was this due to a masking effect, as speculated above, or did BOE attack the black residue itself? A new chip was dipped in BOE for 1 min. The results were most dramatic in the regions of the chip where the O_2 plasma had been unable to remove the black residue. A "lift-off" phenomenon had taken place, removing the black residue by etching the dielectric out from underneath it. This was evident since the chip was not agitated in the BOE and some of the black residue material adhered to the chip surface. But, other regions were still significantly covered with black residue. This confirms the hypothesis that the residue consists of intermixed dielectric and organic residues, each masking the other. The organic residue appears black in color. The chip was then exposed to O_2 plasma (99 sccm, 130 mTorr, 350 Vbias, ~280 W, 40°C) for one hour which removed most of the remaining residue. The fact that the O_2 plasma, with the given parameters, does not roughen the GaAs surface was verified by using it on a bare GaAs wafer. By interleaving BOE (1 min) and O_2 plasma (1 hour) once more, the DGWs were uniformly cleaned, as seen in Figure 3.5.

Thus, the residue in the DGWs consists of dielectric, which is etched by BOE, and fluorinated hydrocarbons, which are etched by O_2 plasma (or ozone). Since the two are intermixed and mask each other, both O_2 plasma and BOE must be employed in the cleaning process.

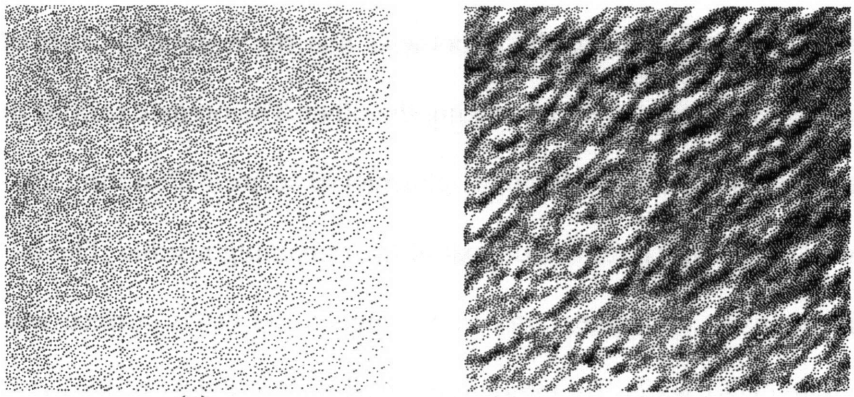
The results seen in Figure 3.5 are unsettling. The GaAs is apparently clean of residues, yet still exhibits a rough morphology. Such a surface is not appropriate for MBE growth.



(a) (b)

Figure 3.5: Nomarski micrographs of DGWs after cleaning with O_2 plasma and BOE. All residue is removed, but GaAs substrate has a rough morphology. (a) 50X, (b) 1000X.

An InGaP based LED was grown on this material, and the morphology of the resulting epitaxy is compared with that produced on bulk GaAs in Figure 3.6. It appears as though



(a) (b)

Figure 3.6: 1000X Nomarski micrographs of InGaP based LED material (a) on a bulk GaAs wafer and (b) in a DGW. The DGW was prepared O_2 plasma and BOE etching. The material in (a) is very smooth, while (b) quite rough.

the rough morphology of the DGW substrate is magnified as it is transferred up to the surface of the epitaxial material. This material may or may not produce working devices, but its presence brings into question the reliability of EoE integration.

3.2 Revised Preparation Method

What is producing the roughness on the DGW substrate? As a baseline for comparison, a piece of "dead" Vitesse substrate (a Vitesse wafer that has gone through the Vitesse process, but only has a partial dielectric stack over it) was cleaned by simply dipping it in pure HF (the entire dielectric stack comes off in less that 1 min. in pure HF). This piece had a featureless morphology, and the epilayer growth on it was identical to the bulk GaAs wafer. The difference between this piece and the DGWs tested is that the underlying GaAs layer of the DGWs was ion implanted (for making a back side contact through a standard Vitesse ohmic contact), and has been exposed to the Vitesse passivation and boundary etches. It may be that the ion implantation processes produces the roughness, but this should have also affected the original growths.

Another speculation as to the cause of the degraded morphology is that the etch used by Vitesse damages the GaAs. This etch is not very precisely controlled, since it is only intended to produce a saw line trench, and it is very vigorous since it must cut through a very thick dielectric stack. However, although some morphology was seen on early growths in the DGWs, this was small in comparison to the roughness seen in the later growths. It is likely that the substrate morphology was much better in the past.

A significant clue as to the origin of the surface roughness is the observation that the black, organic residue is much more difficult to remove once it has come into contact with GaAs [52]. This means that the fluorinated hydrocarbon is reacting with GaAs, which is not surprising due to the high reactivity of fluorine. Certainly, the reaction rate is very slow, but in the course of a year, a significant amount of GaAs is consumed. Since the organic residue is intermixed with dielectric, it interacts with the crystal nonuniformly. When it is finally removed, the reacted GaAs is also removed, producing the rough surface. This model accounts for all observations.

The above model says that the residue from the CF_4/O_2 etch must not be allowed to come in contact with the GaAs. In other words, the Vitesse etch depth must be limited to less than the total dielectric stack thickness. O_2 plasma may be used to remove the organic residue, and BOE may be used to etch the remainder of the Vitesse dielectric. In this case, it will be necessary to mask the remainder of the chip to protect the bond pads from over-exposure to BOE. If the dielectric is not thin enough to allow a controllable isotropic wet etch, CF_4/O_2 RIE may be used to thin the dielectric before the BOE etch. The proposed process is diagramed in Figure 3.7.

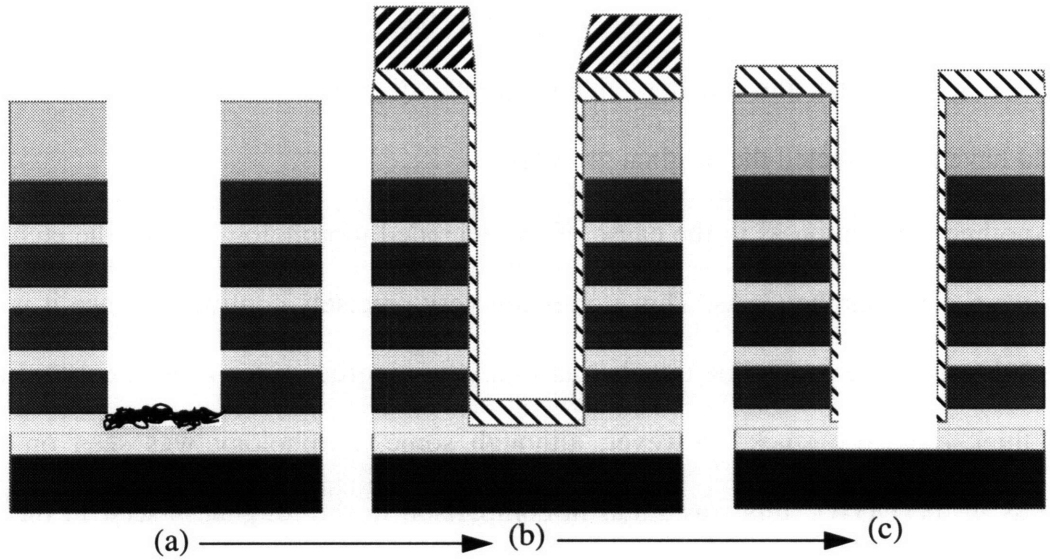


Figure 3.7: Proposed process for DGW preparation. (a) Chips arrive from Vitesse with the DGWs only partially etched. (b) O_2 plasma is used to remove any organic residues. A layer of dielectric is applied to protect the bond pads in post growth processing. Photoresist is patterned to expose the DGWs. (c) CF_4/O_2 is used to thin the dielectric remaining in the DGW if necessary. BOE removes the last thin layer of dielectric to expose a clean, smooth GaAs surface.

In addition to the steps discussed above, a layer of dielectric is to be applied over the entire chip before opening the DGWs. This will protect the aluminium bond pads in the post growth replanarization step in which the polycrystalline material outside the DGW is etched. This layer does not play a critical role in the DGW preparation process.

The DGW preparation method outlined in Figure 3.7, referred to as the "revised" procedure, is to be applied to new sets of chips. Since the boundary etch has been removed from the *normal* Vitesse process, it is possible, by special arrangement, to have it reinserted with a modified etch time/energy. Chips were returned from Vitesse with the dielectric stack partially etched (1-2 μm of dielectric remaining). On these chips, the black residue was much less dense, since less material was etched. Full application of the revised procedure requires a photolithography mask for patterning the photoresist over the regions of the circuit that are to be protected. Since this mask was not yet available, the revised preparation technique was verified by dipping the chip face down in BOE, with ultrasonic agitation. After 30 min. the dielectric stack was completely removed from the DGW areas and a clean, smooth GaAs surface was exposed. The result of this preparation step is shown in Figure 3.8.

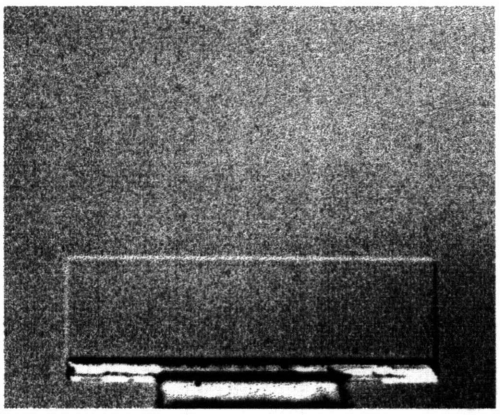


Figure 3.8: 1000X Nomarski micrograph of DGW prepared with the revised method: the Vitesse etch was stopped short of GaAs substrate and remaining dielectric was removed with BOE. Only the bottom portion of the DGW is ion implanted. Both regions are perfectly clean and smooth. The boundary line is due to a depression of approximately 15 nm on the implanted region.

The DGW pictured in Figure 3.8 was partially ion implanted. In the event of reduced epitaxial quality due to substrate roughness caused by ion implantation, the active device grown in this DGW would be on high quality, non-implanted regions and still connected

to the Vitesse ohmic contact through the implanted portion. As seen in Figure 3.8, the implanted and nonimplanted materials have identical morphology, both very good. The boundary line is a result of a roughly 15 nm height difference between the two regions, the implanted region being lower. One explanation for the recession of the implanted region is implantation-induced surface sputtering [53]. Another explanation is that the etch used to define the active areas also attacks the GaAs. Whatever the cause, both regions appear to be suitable for growth.

Growth of AlGaAs based heterostructures on a new chip prepared by etching in BOE has been found to match the high quality material grown on the accompanying bulk GaAs wafer.

In conclusion, a new procedure has been developed for the preparation of DGWs prior to growth. This procedure replaces the original method which failed as a result of damage to the GaAs substrate caused by the reactive organic residues produced by the etch process that was used to define the DGWs. The new procedure protects the substrate by etching only partially through the dielectric stack and then removing the remainder of the dielectric using BOE.

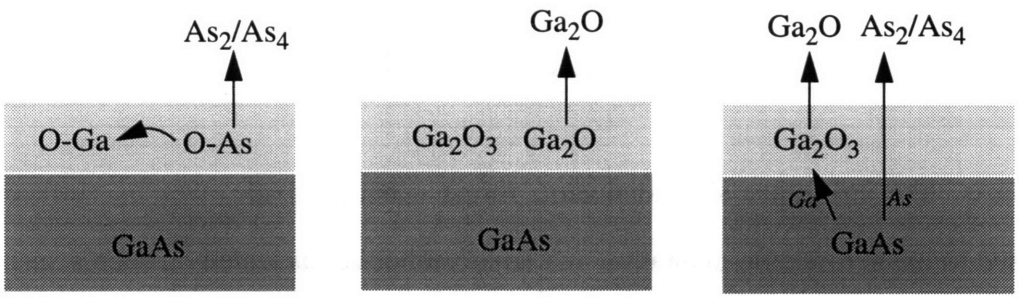
Chapter 4

Low Temperature Oxide Removal

GaAs, like any other semiconductor, forms a native oxide over its surface when exposed to oxygen. Single-crystalline material can not be nucleated on such a surface, so the oxide must be removed prior to growth. In conventional MBE practice, the surface oxide is thermally desorbed by raising the substrate temperature to 580°C-600°C for a short time while maintaining an arsenic overpressure to prevent the loss of arsenic from the crystal (the thermal desorption process is discussed in Section 4.1). However, as discussed in Section 2.1, even a brief exposure to such temperatures is detrimental to the VLSI electronics. Fortunately, as discussed in Section 4.2, an alternate oxide removal technique exists which works at much lower temperatures. Preliminary results using this technique are presented in Section 4.3 and discussed in Section 4.5.

4.1 Background: Thermal Desorption of GaAs Native Oxide

The native oxide of GaAs is composed of As_2O_x (x=1,3, or 5), Ga_2O, and Ga_2O_3. A partial model for the oxide desorption process is sketched in Figure 4.1 [54]. There are three phases in the process, each occurring at different temperatures. The arsenic oxides are the least stable; at 390°C they break down releasing molecular arsenic and allowing the formation of additional gallium oxides. The remaining oxide is composed of Ga_2O_3 and Ga_2O, the latter of which desorbs at 475°C. Above 500°C, a reaction between the underlying GaAs and the Ga_2O_3 produces Ga_2O and molecular arsenic. Once these products have desorbed, the GaAs surface is free of oxides. In all likelihood, this model is largely correct. However, subsequent investigation has indicated the presence of arsenic oxides even after a 410°C exposure [55], though this may simply be due to inaccuracy in determining



(a) T_{sub}=390°C (b) T_{sub}=475°C (c) T_{sub}>500°C

Figure 4.1: Thermal desorption of GaAs native oxide. The oxide layer is composed of As_2O_x (x=1, 3, 5), Ga_2O, and Ga_2O_3. (a) Elimination of the arsenic oxides occurs at 390°C. In this step, additional gallium oxides are formed using oxygen from the arsenic oxides while the arsenic is desorbed as molecular As_2 or As_4. (b) At 475°C the Ga_2O desorbs from the surface leaving only Ga_2O_3. (c) Finally, above 500°C a reaction between the Ga_2O_3 and GaAs produces Ga_2O and molecular arsenic which are desorbed [54].

the substrate temperature.

Whatever the chemical mechanism, it is known that complete desorption of the GaAs oxide at 500°C takes approximately one hour [56]. In practice, the oxide is desorbed above 580°C where it takes one minute [56]. However, since the congruent sublimation temperature of GaAs is around 580°C-640°C [56], high temperature oxide desorption must be carried out in an arsenic overpressure in order to prevent the formation of a gallium-rich surface.

4.2 Background: Removal of GaAs Oxide by Atomic Hydrogen

Although thermal desorption is effective at removing oxygen from the GaAs surface, carbon contamination remains up to 650°C, making it difficult to obtain a very clean starting surface [57]. The presence of carbon results in a high concentration of deep levels, thus decreasing carrier concentration and photoluminescence intensity [57]. Additionally, thermal desorption has been seen to produce surface roughness [58,59]. Motivated by such

issues, significant work has been done in the use of neutral atomic hydrogen (referred to as hydrogen radicals in the literature) for surface cleaning. The source of atomic hydrogen in these investigations has been electron cyclotron resonance (ECR) generated hydrogen plasma [57,60,61,62,63,64,65,66,67,68,69], radio frequency (RF) generated hydrogen plasma [70,71,72], and thermally cracked H_2 [55,73,74,75]. Atomic hydrogen generated using three sources removes oxygen and carbon at substrate temperatures as low as 300°C, and reports of oxide removal even at room temperature have been made [67]. The ability to grow epitaxial material on a hydrogen cleaned surface has been verified by growing GaAs at the conventional temperature of around 580°C following the hydrogen cleaning [57,61,62,63,69,71], as well as growing GaAs at low temperatures using unconventional growth techniques [60].

Two reactions are believed to play a significant role in the removal of GaAs oxide by hydrogen radicals [55]. At 350°C, the reaction $As_2O_x + 2xH \rightarrow xH_2O + As_2$ (or $\frac{1}{2}As_4$), where x=1,3, or 5, removes the arsenic oxide by converting it to water and molecular arsenic, which desorb from the surface. At 410°C, Ga_2O_3 is eliminated through the reaction $Ga_2O_3 + 4H \rightarrow 2H_2O + Ga_2O$ by its conversion to Ga_2O and water, which are also desorbed.

Process parameters vary widely in the literature, and there are conflicting results regarding the nature of the resulting surface. In some cases, it is reported that a 500°C anneal following the hydrogen treatment is needed to achieve good RHEED reconstruction [61,62]. There are also indications that the hydrogen radicals chemically etch GaAs at up to 10 nm/hr (1.7 Å/min) [65,66]. A complete understanding of GaAs oxide removal by hydrogen radicals is clearly not yet in hand. There is good reason, however, to believe that conventional growth, at 470°C, of InGaP and GaAs on a hydrogen treated surface should be possible.

Due to the availability of an RF plasma source, reports of GaAs oxide removal using RF generated hydrogen plasma are of particular interest. One approach was to use a 13.56 MHz plasma discharge free radical source from Oxford Applied Research (Oxfordshire, UK) [70]. Using 320 W of RF power in $4x10^{-6}$ Torr of hydrogen ambient, with possibly some nitrogen content, the GaAs oxide was removed at temperatures of 300°C-400°C based on observation of streaky RHEED patterns. Similarly, $Al_{0.24}Ga_{0.24}As$ (lattice-matched to InP) was cleaned using 500 W of RF power in $2.4x10^{-5}$ Torr of H_2 at 370°C in 22 min. [71]. Another group dissociated H_2 by mixing it with an RF generated Ar plasma [72]. Flowing at a rate of 200-400 sccm, Ar was pumped with 30 W of 13.56 MHz RF power. Downstream from the RF plasma source, 100 sccm of H_2 was added, producing atomic hydrogen. The GaAs substrate was maintained at 350°C. Again, RHEED patterns indicated removal of the oxide in 10-30 s. The authors also reported that hydrogen treatment in excess on 1 min resulted in As depletion and gross surface damage.

4.3 Implementation

The II-VI reactor of the integrated III-V/II-VI Gas Source MBE (GSMBE) system at M.I.T. is equipped with an Oxford Applied Research CARS25 13.56 MHz RF plasma source for the generation of nitrogen radicals for the p-type doping of II-VI films. A high purity H_2 tank and manifold were added to allow investigation of H plasma oxide removal. Generation of H plasma from pure H_2 was found to be impractical due to the high powers required. The pure H_2 was replaced with a H_2/Ar mixture (10% Ar), allowing easy, consistent production of a reactive H plasma.

4.3.1 The Hydrogen Plasma Source

The type of source employed can produce two modes of hydrogen plasma. Low brightness mode (LBM) can exist at any pressure and power, but does not contain a high

enough concentration of excited H_2 or H radicals to produce a significant reaction rate. The high brightness mode (HBM) does produce reactive H, but is more difficult to ignite. A pressure/power hysteresis loop connects the two stable states, so by igniting a LBM plasma and then lowering the pressure, a stable HBM plasma may be attained.

An HBM H plasma is consistently produced with the H_2/Ar source. The basic procedure for operation of the hydrogen plasma source is as follows:

1. The sample is loaded into the II-VI chamber and the substrate heater is ramped to the desired temperature. The chamber is configured to be pumped by the diffusion pump.
2. The flow rate of H_2/Ar is adjusted to set the chamber ambient pressure necessary to strike the plasma in LBM.
3. The RF power is smoothly raised to the desired value (normally 350 W). A LMB plasma should ignite well below this value (normally ~100 W).
4. The chamber pressure is then lowered (by reducing the H_2/Ar flow), until the plasma enters HBM.

4.3.2 ZnSe on GaAs

The nucleation of ZnSe on GaAs is complicated by the heterovalent nature of the crystal bonding between the two. Consequently, the growth of ZnSe on GaAs is very sensitive to the condition of the starting surface. The use of H plasma was investigated as a means of improving ZnSe on GaAs heteroepitaxy by House, *et al.* [76]. Photoluminescence of ZnSe grown on an epitaxial GaAs buffer layer, which is the "ideal" starting surface, is compared with that of ZnSe grown directly on a H plasma treated GaAs wafer in Figure 4.2. The ratio of the free and bound exciton peaks and the lack of a defect band indicate that both samples are of high optical quality. This implies that the H plasma treatment produced an excellent nucleation surface.

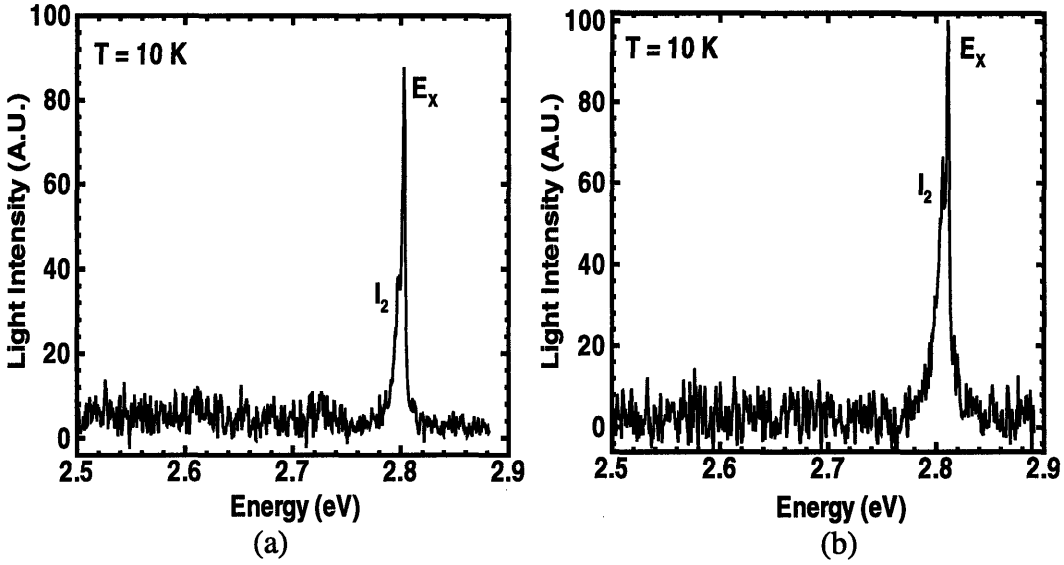


Figure 4.2: Photoluminescence of ZnSe grown on GaAs. The sample in (a) used a hydrogen plasma for oxide removal, while in (b) the sample was grown on an epitaxial GaAs buffer layer (the highest quality starting surface possible). In both cases, the ratio of the intensity peaks of the free (E_X) and donor-bound (I_2) excitonic transitions, and the lack of a defect band, indicate that the quality of the starting surface allowed the growth high optical quality material [76].

4.4 Results

Five trials of hydrogen plasma oxide removal were completed. In this initial investigation, careful refinement of process parameters was not yet possible. Rather, an attempt was made to identify a reasonable point of departure in establishing a repeatable, effective procedure. For simplicity, the five trials are recounted in chronological order. Section 4.5 will draw conclusions from these trials.

4.4.1 Trial 1 (Growth R195)

Cleaved pieces of an n^+ GaAs wafer were In mounted, baked for 1 hour at 210°C, and loaded into the II-VI chamber for hydrogen plasma cleaning. The H plasma parameters are given in Table 4.1. The diffuse RHEED pattern characteristic of an oxide covered GaAs surface is shown in Figure 4.3. In this run, the RHEED pattern remained diffuse during the

Pressure (Base)	9.4×10^{-7} (2.3×10^{-8}) Torr
Power	350 W
$V_{brightness}$	4.2 V
$T_{substrate}$	300°C
Time	57 min

Table 4.1: H-Plasma Parameters for R195

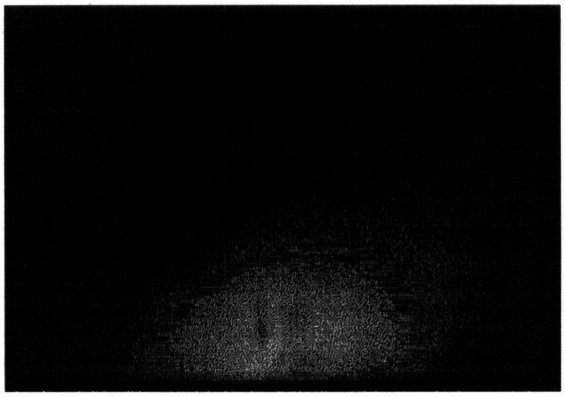
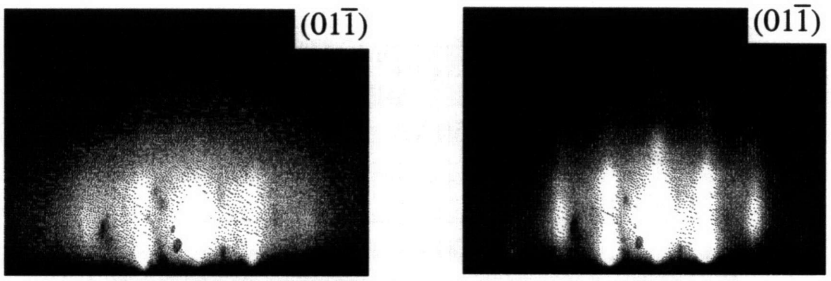


Figure 4.3: Diffuse RHEED pattern of oxide covered GaAs.

first 20 min of H plasma exposure, at which time faint spots began to appear. These spots gradually became more defined. After 35 min of H plasma exposure, definite streaks are visible (Figure 4.4(a)), indicating elimination of the surface oxide. The sample was left in plasma for a total of 57 min.; the final RHEED image is shown in Figure 4.4(b).

The sample was next transferred into the III-V growth chamber. The substrate temperature was ramped to the growth temperature, 470°C, with As overpressure being applied when the substrate reached 300°C. Just prior to growth, the RHEED pattern remained streaky. Growth was nucleated by opening the Ga and Si shutters. The RHEED pattern immediately became spotty, indicative of bulk diffraction and thus a very rough surface.



(a) t=35 min (b) t=57 min

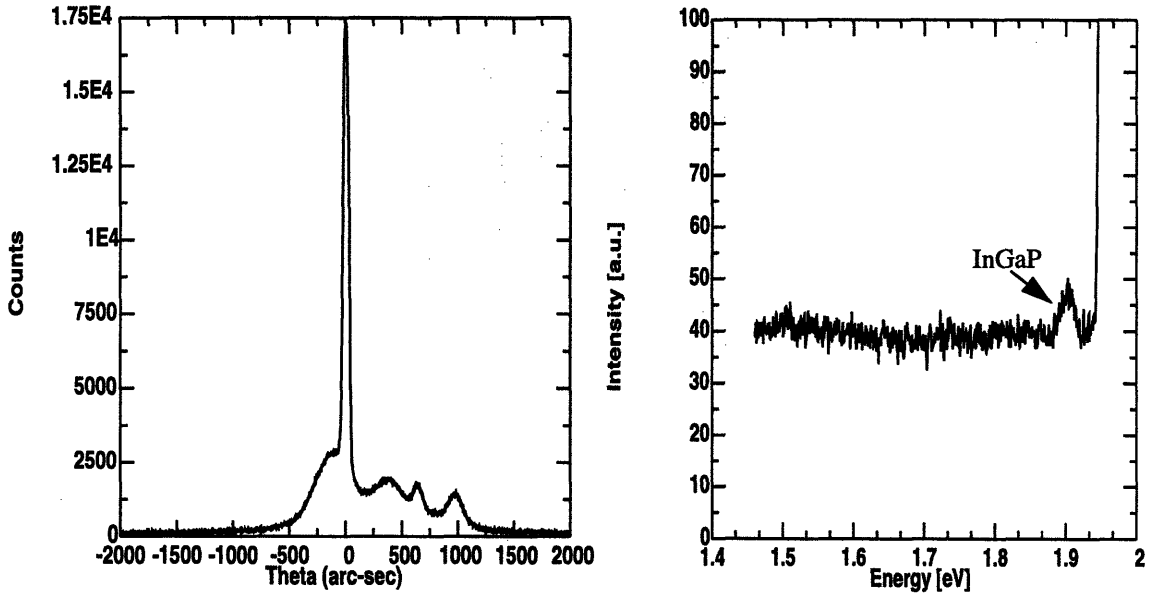
Figure 4.4: RHEED patterns from R195 H plasma trial. (a) are after 35 min. exposure. (b) are after 57 min. exposure.

By stopping the growth and annealing the sample, a somewhat streaky, 2-D RHEED pattern was recovered. In fact, the RHEED pattern at the completion of an LED structure was indicative of a reasonably good crystalline surface. However, double crystal x-ray diffraction (DCXRD) indicates very poor material quality and photoluminescence (PL) shows no emission for the GaAs active layer (Figure 4.5).

4.4.2 Trial 2 (R196)

The results of R195 indicated that the surface may have been roughened during the oxide removal process, perhaps as observed in [72]. Under this assumption, the H plasma exposure was terminated as soon as distinct streaks appeared in the RHEED pattern. In addition, it was speculated that Ga did not have a high enough surface mobility at 470°C to overcome the surface roughness. Since In has a higher surface mobility at the low temperature, it was hypothesized that growth nucleation with InGaP would recover a 2-D growth surface.

A cleaved piece of an n^+ GaAs wafer was In mounted, baked for 1 hour at 210°C, and loaded into the II-VI chamber for hydrogen plasma cleaning. The H plasma parameters are given in Table 4.2. In this run, the RHEED pattern remained diffuse for 12 min of H



(a) (b)

Figure 4.5: (a) DCXRD from R195: LED structure grown on H plasma prepared GaAs. The material is of very low quality. (b)10 K PL from R195. Lack of emission from the GaAs core confirms poor material quality. PL was generated with a He:Ne pump laser, which is seen at the far right of the spectrum.

Pressure (Base)	8.9×10^{-7} (1.8×10^{-8}) Torr
Power	350 W
$V_{brightness}$	4.2 V
$T_{substrate}$	320°C
Time	17 min

Table 4.2: H-Plasma Parameters for R196

plasma exposure. After 17 min of H plasma exposure, definite streaks were visible in the RHEED pattern (Figure 4.6), presumably indicating elimination of the surface oxide.

The sample was next transferred into the III-V growth chamber. The substrate temperature was ramped to the growth temperature, 470°C, with As overpressure being applied when the substrate reached 300°C. Just prior to growth, the RHEED pattern remained

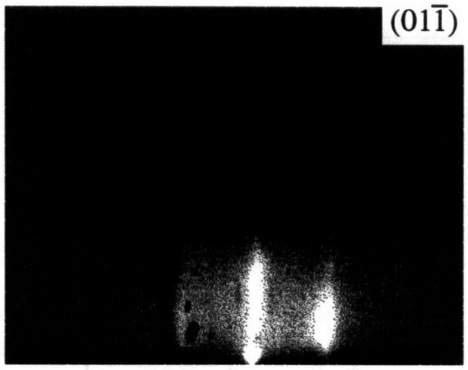


Figure 4.6: RHEED patterns from R196 H plasma trial after 17 min. exposure.

streaky. The overpressure was switched to P, and growth was nucleated by opening the In, Ga, and Si shutters. In this case, growth was nucleated successfully, and the RHEED pattern remain good throughout the growth (other technical difficulties limited the quality of final film). RHEED patterns throughout the growth are presented in Figure 4.7

DCXRD indicates reasonably good material quality and photoluminescence (PL) shows optical emission from the GaAs active layer (Figure 4.8). As discussed in Section 6.2, this sample also produced efficient electroluminescence.

4.4.3 Trial 3 (Growth R252)

The success of R196 indicated that perhaps a higher substrate temperature during the oxide removal was beneficial. The substrate temperature was thus increased to 350°C during the oxide removal procedure. To ensure that the oxide in the dielectric growth wells (DGWs) on the accompanied IC was also removed, the time for the plasma exposure was chosen to be roughly twice the time at which a 2-D (streaky) RHEED pattern was generated by the bulk GaAs wafer.

A cleaved n^+ wafer and a transceiver IC were In mounted, baked, and loaded into the II-VI chamber for H plasma treatment. The plasma parameters are summarized in Table 4.3. The oxide removal process proceeded as in R196, but new effects were seen once the

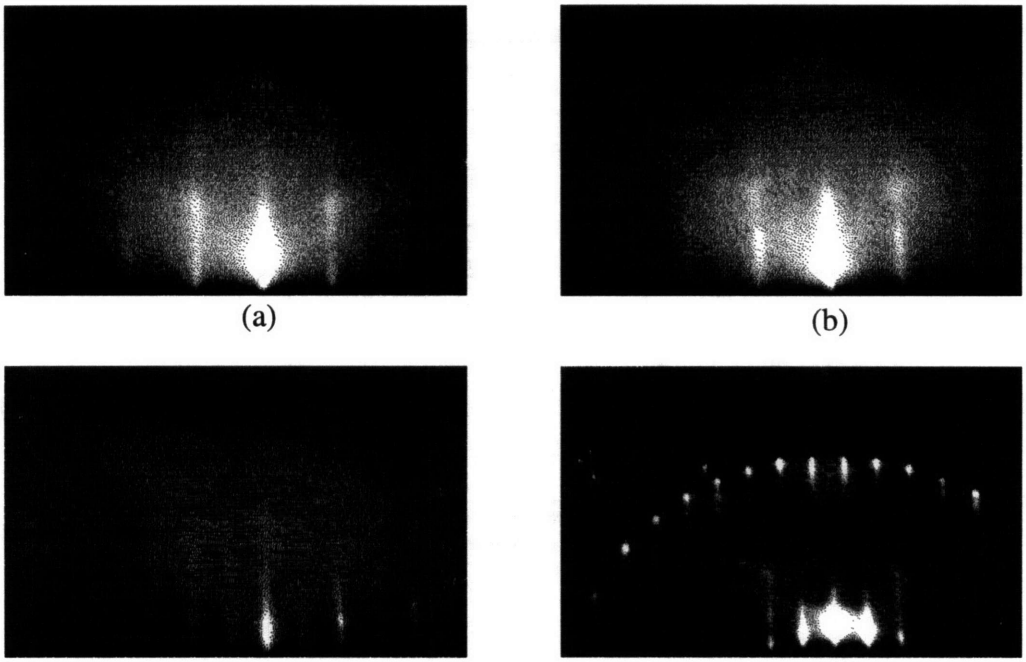


Figure 4.7: RHEED patterns from R196 H plasma trial. (a) After sample is transferred to III-V chamber and substrate temperature is raised to 470°C under As overpressure. (b) Shortly after nucleation of InGaP, a 2-fold reconstruction is visible. (c) During a growth interruption following 2.3 μm of InGaP. (d) GaAs cap layer after completion of entire 3.7 μm LED structure.

Pressure (Base)	4.5×10^{-7} (10^{-8}) Torr
Power	350 W
$V_{brightness}$	2.6-3.3 V
$T_{substrate}$	350°C
Time	40 min

Table 4.3: H-Plasma Parameters for R252

sample was moved to the III-V chamber: When As overpressure was applied, at 300°C, the RHEED pattern became very spotty. At 470°C, growth of InGaP was initiated. The RHEED pattern remained spotty for 30-50 seconds, then recovered to a streaky InGaP RHEED pattern. However, after less than ten minutes of growth, the pattern began to look

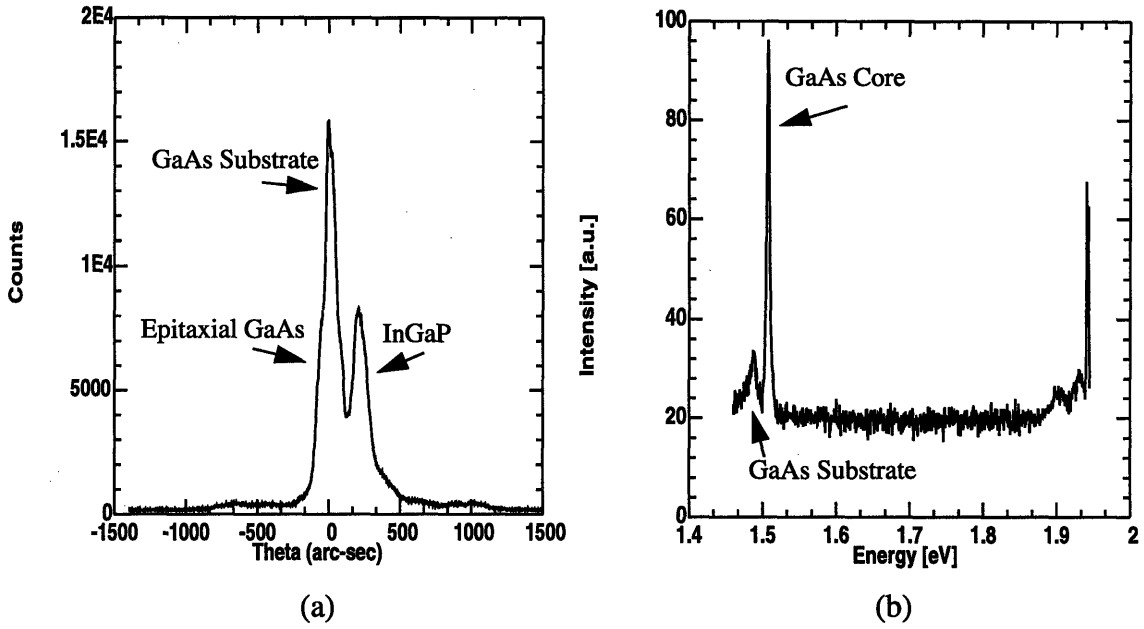


Figure 4.8: (a) DCXRD from R196: LED structure grown on H plasma prepared GaAs. The epitaxial GaAs and InGaP peak widths are only slightly wider than the bulk GaAs, indicating reasonably high material quality. (b) 10 K PL from R196. Optical emission from the GaAs core confirms good material quality. PL was generated with a He:Ne pump laser; this line appears at the far right.

spotty again, and eventually became very spotty and dim, indicating a rough surface. The DCXRD results for this sample are indicative of an extremely high density of dislocations (Figure 4.9(a)).

4.4.4 Trial 4 (Growth R254)

Since R252 used a higher substrate temperature, the surface may have been depleted of As. R254 returned the substrate temperature to 320°C, the value used in R196. A sample was mounted, baked, and loaded as usual. Table 4.4 shows the H plasma parameters. The treatment was stopped once RHEED produced the pattern in Figure 4.10. The exposer time and RHEED pattern agree with those of R196. The pattern remained the same in the III-V chamber, but when the sample was raised to 300°C and As was applied, the RHEED pattern again became very spotty, as shown in Figure 4.11(a). Then, with the sample at

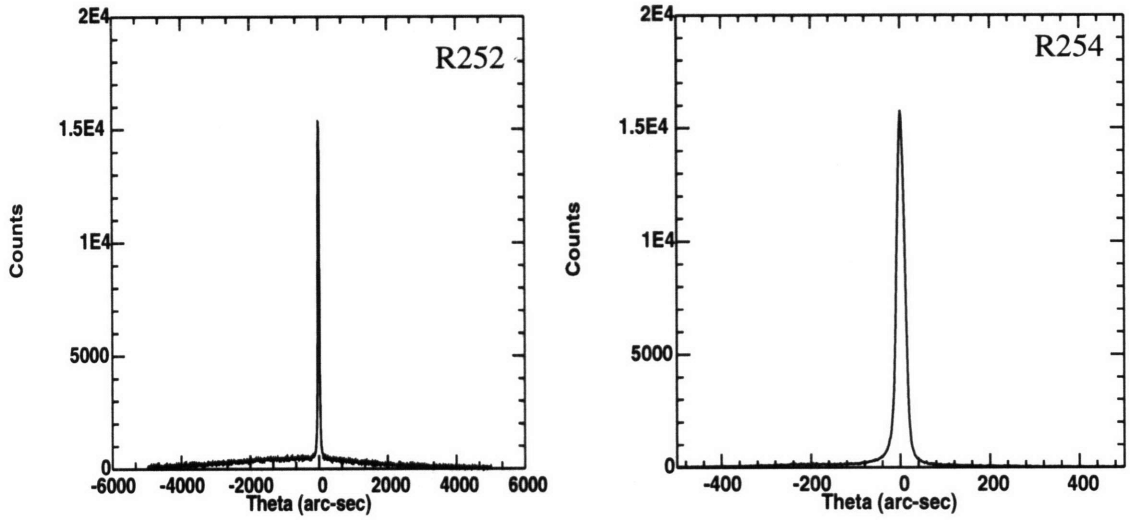


Figure 4.9: (a) DCXRD from R252: LED structure grown on H plasma prepared GaAs. (b) DCXRD from R254: Approximately 0.25 μm of InGaP on H plasma prepared GaAs. Both films contain an extremely high density of dislocations.

Pressure (Base)	$6x10^{-7}$ (10^{-8}) Torr
Power	350 W
$V_{brightness}$	3.5-3.6 V
$T_{substrate}$	320°C
Time	16 min

Table 4.4: H-Plasma Parameters for R254

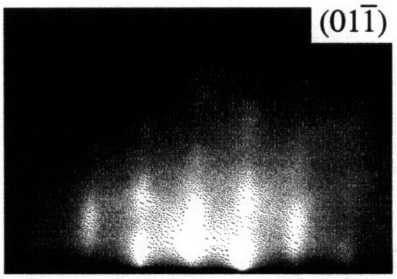


Figure 4.10: RHEED patterns from R254 H plasma trial after 16 min. exposure.

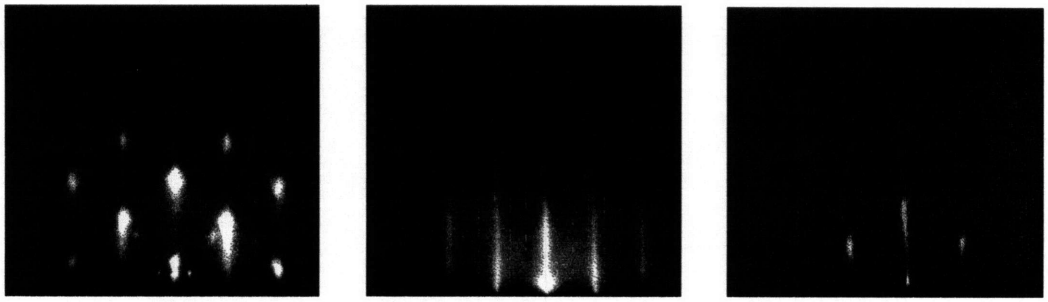


Figure 4.11: RHEED patterns from R254 H plasma trial. (a) In the III-V chamber at 300°C under As overpressure. (b) After increasing substrate temperature to 470°C. (C) After 15 min of InGaP growth.

470°C, the RHEED pattern recovered to a 2-D diffraction pattern, as in Figure 4.11(b). Growth of InGaP was initiated and proceeded smoothly, but after around fifteen minutes, the RHEED pattern again became spotty (Figure 4.11(c)). Growth was terminated at this point. The DCXRD in Figure 4.9(b) again show the material to contain an extremely high dislocation density. The surface morphology is pictured in Figure 4.12. The surface defects resemble those generated by dust specks, but are far more dense than normally experienced.

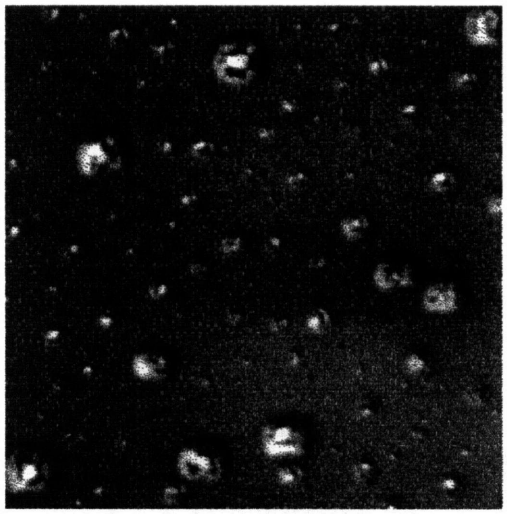


Figure 4.12: 1000X Nomarski micrograph of R254 surface. After H plasma oxide removal, 0.25 μm InGaP was grown.

Pressure (Base)	$7x10^{-7}$ ($5X10^{-9}$) Torr
Power	350 W
$V_{brightness}$	3.8 V
$T_{substrate}$	300°C
Time	22 min

Table 4.5: H-Plasma Parameters for R261

Ga	45.1%
As	49.7%
C	2.0%
O	3.3%

Table 4.6: AES results R261 after H plasma oxide removal

4.4.5 Trial 6 (Growth R261)

The poor results of R252 and R254 tend to indicate that the surface oxide was not completely removed, in spite of indications from RHEED to the contrary. R261 tested this hypothesis by repeating the plasma treatment of R254 and following it by Auger Electron Spectroscopy (AES) to determine the surface composition. The substrate temperature during oxide removal was also lowered but this did not appear to make a significant difference in removal time or growth behavior.

The sample was prepared and treated as before. The plasma parameters are given in Table 4.5. The RHEED pattern after the treatment was identical to the previous cases, in which the oxide was believed to have been removed. In fact, AES showed that the surface composition included 3% oxygen (Table 4.6).

In spite of the presence of surface oxide, the sample was transferred to the III-V chamber for growth. The sample behaved similarly to R254 prior to growth. Rather that conventional nucleation of InGaP, GaAs was grown on a monolayer by monolayer basis. While maintaining As overpressure, the Ga and Si shutters were opened for 5 s intervals, corresponding to 1-2 monolayers. Growth was interrupted for a few minutes between intervals. Oscillations of the RHEED intensity were clearly visible, by eye, for the first six intervals. Beyond this point, oscillations could not be seen by eye, and by the tenth interval the RHEED pattern was getting spotty.

The only clear conclusion that can be drawn from this is that the presence of a non-diffuse RHEED pattern does not indicate complete removal of the GaAs native oxide.

4.5 Discussion

Two significant conclusions can be reached from the five trials: good quality material can be grown on GaAs after using hydrogen plasma to remove the native oxide, and a non-diffuse RHEED pattern does not indicate complete removal of the oxide.

The first point is clearly verified by R196, which produced efficient electroluminescence results. The second point is seen in R261, and an explanation for why this occurs is as follows: if the oxide was being removed nonuniformly, so that some crystal was exposed amidst "islands" of oxide, then RHEED can still produce a streaky pattern. Since the breadth of the electron beam is hundreds of microns (macroscopic on the size scale of the crystal), such a surface would produce a RHEED pattern that is the superposition of the sharp contribution from the crystal and a diffuse contribution from the oxide. This would appear as a streaky RHEED pattern with poor, diffuse contrast, but this lack of contrast is difficult to judge by eye or to quantify.

The results of the other trials, however, are more difficult to interpret. There is a difference between R195, a one hour exposure, and R252, R254, and R261, which were significantly shorter. The poor quality of R195 may be attributed to a rough starting surface, but it seems unlikely that R254 and R261 were similarly roughened since plasma treatment was not extended after seeing a streaky RHEED pattern. R261 suggests that the effects seen in R252 and R254 were due to the presence of a surface oxide. R261 showed the same spotty RHEED following growth nucleation as R252 and R254, and it is known to have had some oxide coverage. The comparison is not conclusive since growth was nucleated differently.

Suppose the residual surface oxide was not uniform, but rather speckled across the GaAs surface in the form of small islands. If, in addition, some of the As had been depleted, leaving the GaAs somewhat Ga rich, then when the As overpressure was applied, stoiciometric GaAs would be formed. At such a low temperature (300°C) the surface mobility is too low to smoothen the surface. The GaAs surface thus becomes rough, resulting in the spotty, 3-D RHEED pattern. Then, when the sample is heated, the surface mobility increases and the surface is able to smooth out, producing a 2-D RHEED pattern. This explains the transient nature of the spotty RHEED pattern observed when R252, R254, and R261 were placed under As overpressure at 300°C.

Now, when growth is initiated, polycrystalline GaAs is deposited on the oxide islands. A spotty RHEED pattern is produced by a rough, polycrystalline material, and this pattern coincides spatially with the streaky pattern generated by the single crystal, and thus obscures it. The small specks of surface oxide nucleate polycrystalline material in the same manner as dust specks. This explains the surface morphology of R254 on which a very high density of dust-like defects is found.

4.6 Further Investigation

The investigation of hydrogen plasma oxide removal in this thesis is of a preliminary nature. In the absence of accepted operating conditions, a broad parameter space was sampled in order to establish a starting point. A much more systematic investigation is required to fully understand the procedure and to establish the repeatability of the results. If surface roughening is indeed an issue, an end point condition must be identified.

The use of the RF plasma source in the II-VI chamber complicated the investigation. To continue the work, a thermal H_2 cracker will be added to the III-V chamber. It is possible that this type of source is more gentle than the RF or ECR plasma sources, meaning that the samples may be overexposed to the treatment to ensure complete oxide removal without fear of surface damage. Also, the effect of As overpressure during oxide removal may be investigated.

Chapter 5

Epi-on-Electronics Compatible Material Growth

5.1 Growth Procedures

5.1.1 Sample Preparation

The basic principles of material growth by molecular beam epitaxy are presented in Appendix A. The present section summarizes, in general terms, the procedures for sample preparation and growth used in this investigation.

All of the substrates used were two inch "epi-ready" n^+-GaAs:Si from American Crystal Technology. The epi-ready designation means that no degreasing or etching of the wafer is needed before use.

Two inch wafers were cleaved into quarters and the unused stored in an evacuated canister for later use. One or two quarter wafers may be mounted for growth, using indium solder, onto a clean two or three inch silicon wafer. The two different sized silicon wafers fit into two different sample blocks. On early runs (prior to R195), Riber three inch indium free blocks were used. Growths after and including R195 used a two inch indium free block designed for the II-VI reactor. This allowed samples to be loaded into the II-VI chamber for hydrogen plasma oxide removal. For subsequent transfer into the III-V chamber, a specially designed "transfer block" allowed the II-VI block to be mated with the III-V transfer arm and manipulator.

The three inch Riber block was loaded directly into the intro-chamber of the III-V reactor. This method did not allow the samples to be outgassed prior to being introduced into the III-V reactor. Use of the II-VI block allowed the samples to be transferred through a load-lock chamber, and a baking stage in the transfer chamber allowed these samples to

be outgassed to reduce residual impurities, such as water, and prevent their entrance into the growth chamber. Samples were baked for one hour at 210°C.

5.1.2 Growth

The flow of liquid nitrogen through the growth chamber's cryo shroud is initiated at the beginning of a growth run. Once the chamber is cold, the effusion cells that are to be used are ramped up to their outgas temperatures, which is generally slightly greater than the temperature used during growth, to drive off impurities. Flux measurements are made on group-III cells at various temperatures. Flow of arsine (AsH_3) and phosphine (PH_3) is initiated next. The flow rates of each gas is controlled by a precision mass flow controller. Both gases are then injected through a thermal cracker at 900°C. This produces arsenic and phosphorus dimers, which provide group V overpressure during growth, and sub-hydride species of AsH_3 and PH_3.

The sample is ramped to 300°C before AsH_3 is switched into the chamber through the cracker. When thermally desorbing the GaAs native oxide, the sample is ramped to 600°C. Around 580°C, the oxide begins to desorb rapidly. On samples containing a GaAs buffer layer, growth of GaAs is initiated at 600°C, and the substrate is ramped back down to 470°C for the remainder of the growth. Samples that did not use a GaAs buffer layer, but rather an InGaP layer grown directly on the substrate surface, were ramped to 470°C immediately after thermal desorption of the oxide. The corresponding procedure used in hydrogen plasma oxide removal experiments is given in Chapter 4.

The growth rates used were nominally 0.4 or 0.5 μm/hr. for both InP and GaAs. The Si and Be cell temperatures were set to yield doping levels of around $10^{18}/cm^3$.

Once the desired material layers have been grown, the substrate temperature is lowered to 100°C. The arsine overpressure is removed at 350°C.

Particular attention must be paid to InGaP/GaAs interfaces. If an InGaP surface is left under an As overpressure for more that approximately 3-5 seconds, arsenic begins to displace the phosphorus at the surface. As this occurs, the RHEED patterns becomes spotty, indicating a3-D surface. The pattern returns to a streaky, 2-D pattern once GaAs in grown for a few seconds. The ultimate effects of phosphorus displacement at the surface is not yet clear.

5.2 Material Quality

The quality of InGaP, GaAs, and InGaAs, grown at 470°C, have been investigated by double crystal x-ray diffraction (DCXRD) and photoluminescence (PL).

5.2.1 InGaP

Unlike AlGaAs, which is essentially lattice-matched for any Al mole fraction, InGaP is only lattice-matched to GaAs at $In_{0.49}Ga_{0.51}P$. Deviation from this composition results in lattice strain. If the layer thickness of a strained material exceeds a critical value, then a large density of dislocations, which act as nonradiative recombination centers, are produced. In the laser and LED structures, InGaP layers of up to 2.3 μm thick are used. To achieve high InGaP quality, the InGaP composition must be controlled to within one percent.

A DCXRD curve from a high quality GaAs/InGaP double heterostructure (R245) is shown in Figure 5.1. R245 is an LED heterostructure consisting of a 2.3 μm of InGaP:Si bottom cladding grown directly on the GaAs substrate, followed by a 0.6 μm GaAs core, a 0.7 μm InGaP:Be top cladding, and a 0.1 μm GaAs:Be contact layer. The InGaP and GaAs peaks are very closely spaced, indicating that InGaP was nearly perfectly lattice-matched to the GaAs. The narrow full-width at half maximum (FWHM) of the peaks verifies the high crystalline quality of this lattice-matched material.

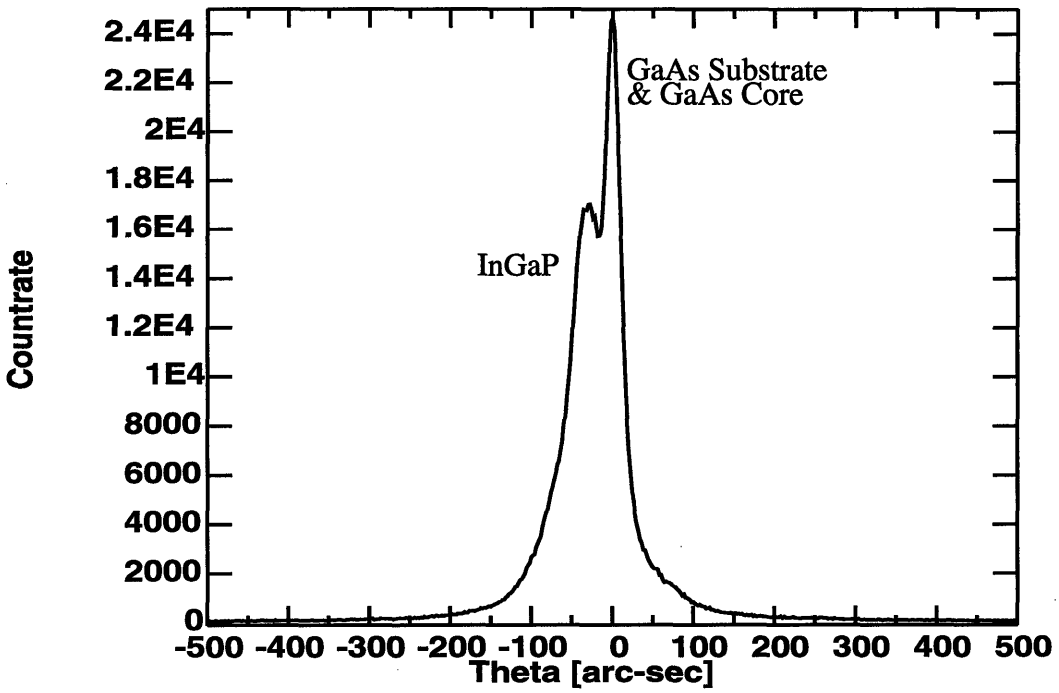


Figure 5.1: DCXRD curve for R245. The near overlap of the InGaP and GaAs peaks means that the material are almost exactly lattice matched. The roughly 50 arc-sec FWHM of the InGaP peak is comparable to that of the combined GaAs core and substrate peak.

Lattice-matched $In_{0.49}Ga_{0.51}P$ has a bandgap of 1.9 eV at room temperature and 2.0 eV at 10 K. This means that it is not excited by a 1.959 eV He:Ne pump laser used in PL measurements, and is not seen in Figure 5.2. The other available pump laser, a UV emitting He:Cd laser, was absorbed by the GaAs cap layer and also did not pump the InGaP. However, a 4 μm film (sample R83) of $In_{0.5}Ga_{0.5}P$, having 272 arc-sec separation between the InGaP and GaAs substrate DCXRD peaks, was excited by the He:Cd pump laser and had a PL peak FWHM of 8.8 meV [77].

5.2.2 GaAs

As seen in Figure 5.1, the GaAs core and GaAs substrate peaks are indistinguishable. Within the resolution of this measurement, the GaAs crystalline quality is comparable to that of the substrate.

The optimal growth temperature of GaAs is around 580°C. At 470°C, the reduced Ga surface mobility may limit the optical quality of the GaAs. However, as seen in Figure 5.2, the PL from the 470°C grown GaAs core of the LED heterostructure of R245, exhibited a FWHM of 5 meV. The high quality of this GaAs is further corroborated by the LED

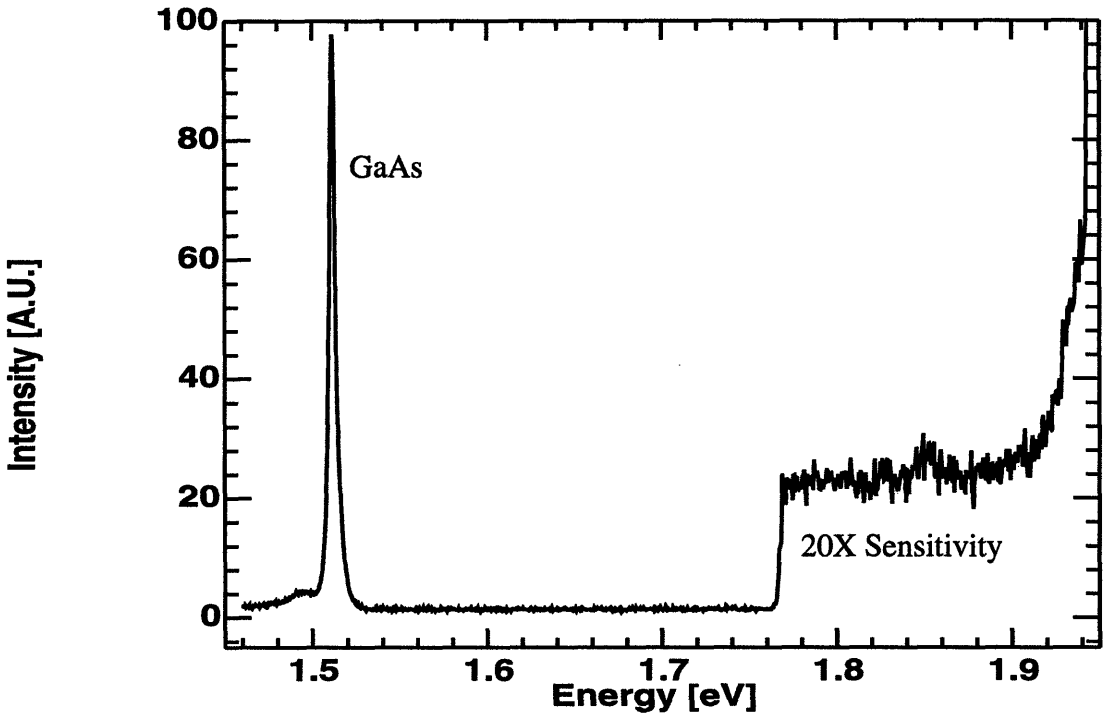


Figure 5.2: 10 K PL of R245 LED heterostructure. A FWHM of 5 meV for the GaAs peak indicates that high optical quality GaAs can be grown at 470°C. A He:Ne pump laser was used to excite the sample, and can be seen at the far right of the spectrum.

results presented in Chapter 6.

5.2.3 InGaAs

To characterize the growth of InGaAs/GaAs quantum wells at 470°C, a test structure consisting of an InGaAs quantum well at the center of a GaAs p-i-n diode was prepared (R161). Based on RHEED intensity oscillation data, the quantum well was 69 Å of $In_{0.3}Ga_{0.7}As$. A DCXRD curve is shown in Figure 5.3. The presence of interference

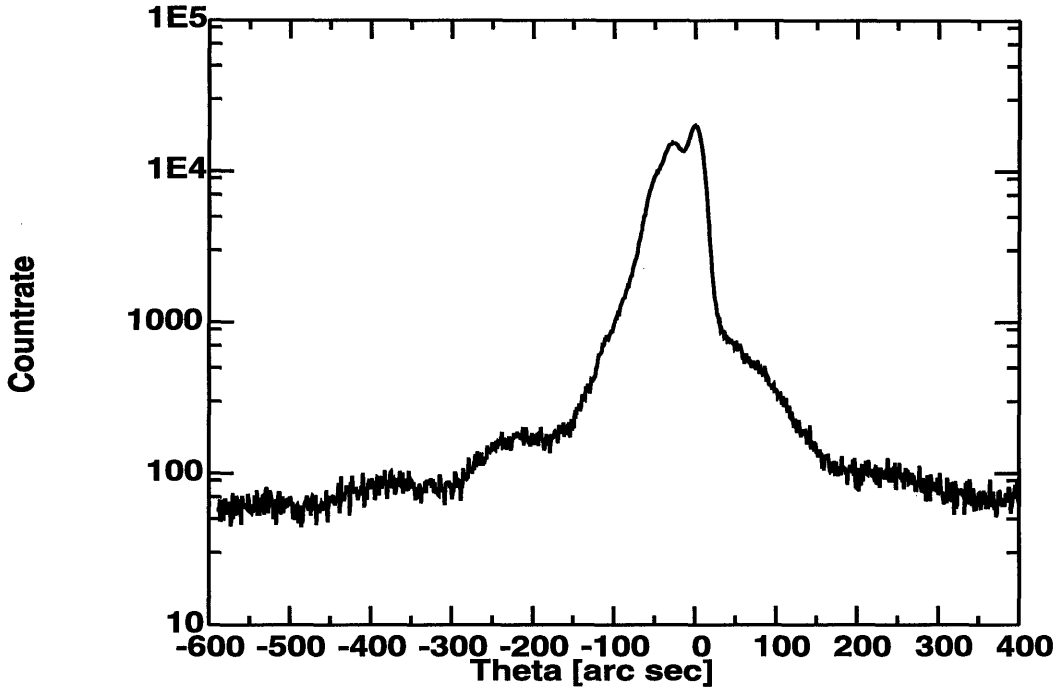


Figure 5.3: DCXRD curve for R161: 69 Å $In_{0.3}Ga_{0.7}As$/GaAs quantum well grown at 470 °C. The interference fringes to the side of the GaAs and InGaAs peaks indicate the formation of abrupt InGaAs/GaAs interfaces.

fringes to the side of the InGaAs and GaAs peaks indicate the formation of abrupt quantum well interfaces.

The R161 quantum well 10 K PL emission was beyond the spectral range of the available low temperature PL measurement setup. A room temperature PL spectrum made on another apparatus is shown in Figure 5.4. The FWHM of the quantum well and GaAs PL peaks are consistent with thermal broadening. Theoretical values for the allowed interband quantum well transitions are in agreement with the observed spectrum.

5.2.4 Conclusion

In conclusion, InGaP, GaAs, and InGaAs have been found to exhibit good crystalline and optical properties when grown at 470°C by gas source MBE. The performance of LEDs and laser diodes based on these materials will be examined in Chapter 6 and Chapter 7, respectively.

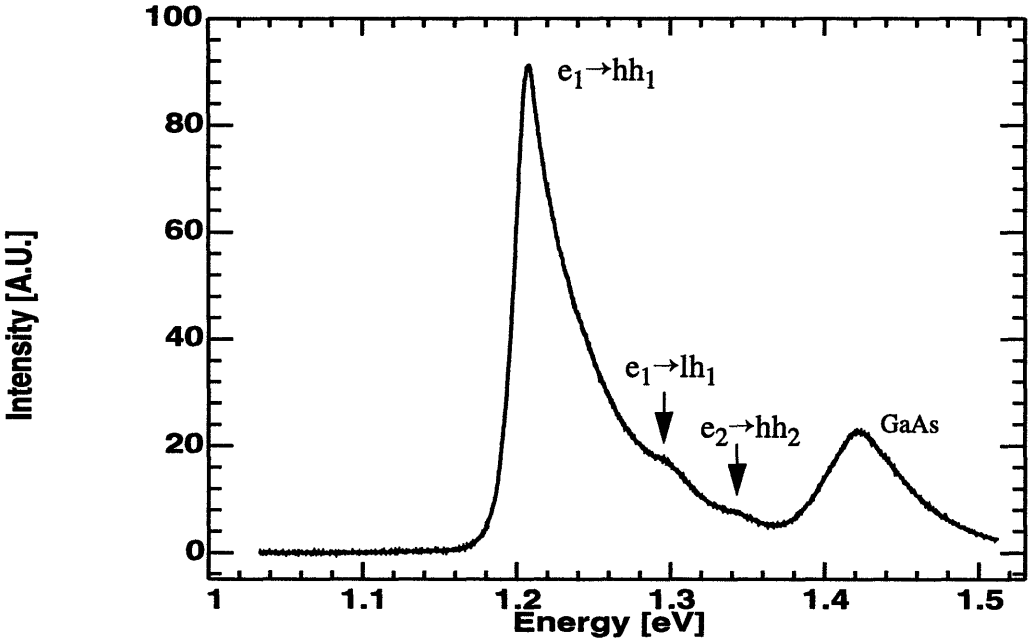


Figure 5.4: 300 K PL of a compressively strained $In_{0.3}Ga_{0.7}As/GaAs$ 69 Å quantum well grown at 470°C (R161). The FWHM of around 50 meV for the dominant peaks is consistent with thermal broadening. The indicated quantum well transitions are in agreement with theoretical energy level calculations. The sample was excited by an Ar^+ pump laser.

Chapter 6

Light Emitting Diodes

Light emitting diodes are an attractive light source for optical interconnect applications that do not require high optical power. Laser diodes have significant light output only for currents above a threshold. Below threshold, a laser has a vanishing efficiency, which means that power must be spent in order to reach laser threshold with no return in terms of optical output. Since LEDs do not have a threshold, low optical output powers can be produced more efficiently than with a laser. However, lasers are very efficient above threshold, and readily overtake LEDs as more current is applied. Thus, the efficiency of the LED determines the operating range over which it is useful. This chapter explores EoE compatible growth of LED material.

6.1 Background

6.1.1 Efficiency

LED efficiency is defined as the optical power extracted per unit terminal current, $\eta=P_{out}/I$. The efficiency of an LED is hampered by nonradiative recombination. The current through an LED is the sum of radiative and non-radiative components. The radiative current varies with voltage as $e^{eV/kT}$ whereas the nonradiative current varies as $e^{eV/2kT}$ [78,79]. On a plot of log(I) vs. V, the radiative current varies with twice the slope of the nonradiative current. For very low voltages, the nonradiative current is larger than the radiative current. For a large enough voltage, however, the radiative current will exceed the nonradiative current. At this point, a "kink" is observed in the log(I) vs. V curve. The current at which this kink occurs is indicative of the density of nonradiative recombination centers. Above the kink, radiative current dominates the total current, and a dramatic increase in η is observed.

6.1.2 AlGaAs-Based LEDs

As a point of reference, results pertaining to fully processed, EoE integrated LEDs based on a GaAs/AlGaAs double heterostructure (DH) are presented. These devices are representative of AlGaAs-based LEDs optimized for EoE integration. The device geometries are sketched in Figure 6.1. Table 6.1 summarizes the relevant device dimensions and gives operating parameters at 1 mA terminal current. The output power efficiency is plot-

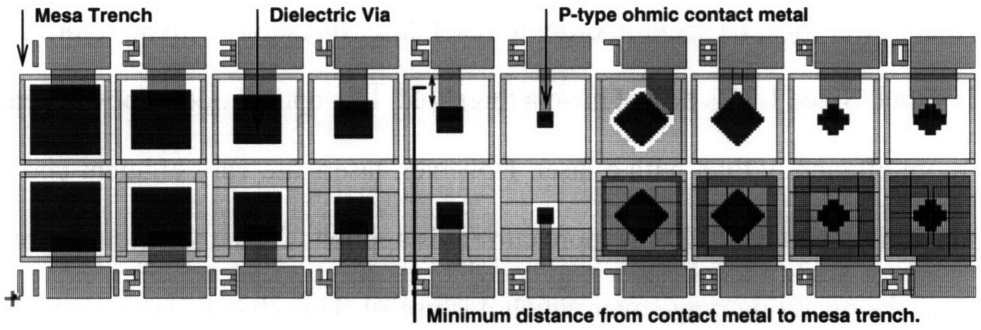


Figure 6.1: Layout of LED device structures fabricated from a GaAs/AlGaAs double heterostructure on a Vitesse IC. LEDs 1 through 6 on the left hand side of the upper row were tested. A mesa trench defines a 30 μm square mesa. The contact size and distance from the mesa edge of each of the annealed Au/Zn ohmic contacts is tabulated in Table 6.1 [80].

LED #	Optical Power [nW]	Efficiency $x10^{-6}$ [W/A]	Contact Area [μm^2]	Current Density [KA/cm^2]	Min. Dist. Cont. to Mesa. [μm]
1	5.26	5.26	80	1.25	2.0
2	17.43	17.43	70	1.43	4.0
3	21.20	21.20	60	1.67	6.0
4	19.51	19.51	50	2.00	8.0
5	38.60	38.60	40	2.50	10.0
6	101.70	101.70	12	8.33	12.0

Table 6.1: EoE integrated GaAs/AlGaAs LED device dimensions and operating characteristics. The device layout is shown in Figure 6.1. The devices are being operated at 1 mA [80].

ted as a function of terminal current in Figure 6.2 [80]. The power generated at 1 mA by

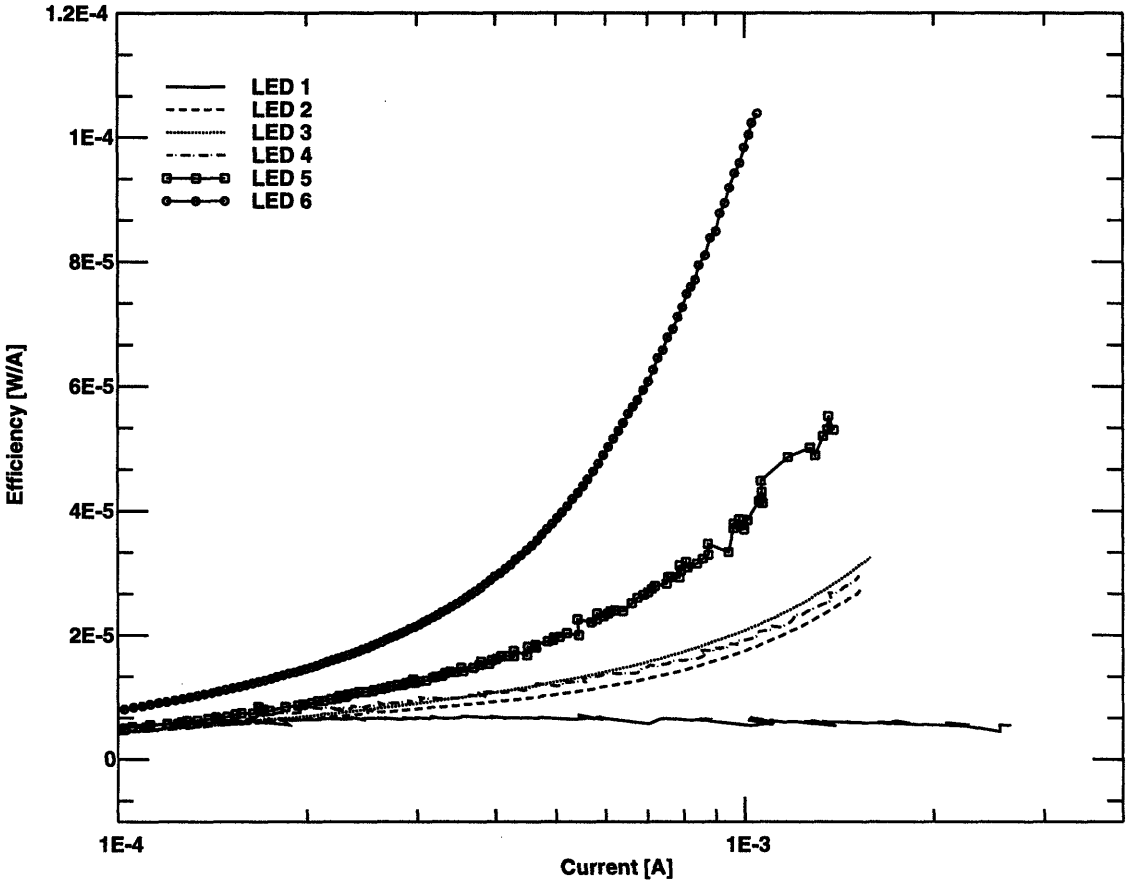


Figure 6.2: Output power efficiency for fully processed, integrated GaAs/AlGaAs LEDs. The device geometries for each led are pictured in Figure 6.1 [80].

LED#6, the most efficient of the set, is adequate for some applications. However, a 1 mA current is above the threshold of some lasers, so that the advantage of threshold-less operation is not being realized. The goal of this chapter is to develop material for higher efficiency LEDs.

6.1.3 Test Structure

The test structure used to characterize the LED material in this thesis consists of a 500 μm diameter spot of Cr/Au ohmic metallization evaporated onto the surface of the sample

through a shadow mask. The sample is thinned by lapping and a back side Cr/Au contact is evaporated. This type of structure may rightly be termed a "broad area" LED. Due to the large contact area, the current density through the device is well known, however the broad area contact also blocks most of the light that is generated. Only light that is emitted around the perimeter of the contact is extracted. The current that generates this light is due to current spreading. Thus, the current density involved in generating detectable light is a fraction of the current density under the contact.

Consider a contact of radius l, and suppose that the current spreads laterally by a distance d. Then, the total area pumped is $\pi(l+d)^2$, while the area that is blocked by the contact is πl^2. Thus, the fraction of the pumped area that produces extractable light is

$$\frac{\pi (l+d)^2 - \pi l^2}{\pi l^2} \approx 2\frac{d}{l} \tag{6.1}$$

If current crowding effects are ignored, the lateral spreading distance depends on the conductivity of the upper cladding of the LED material and its thickness. Its dependence on the contact size, l, is a higher order effect. Thus, d can be assumed constant as l is scaled, even down to the dimensions of the LED structures in Figure 6.1. As l is reduced from 500 μm to 5 μm, the extraction efficiency is expected to increase by a factor of 100. More precisely, since one side of the contact in the processed LEDs is not exposed, the ratio of the extraction efficiencies of the fully processed and broad area LED structures is around 75.

6.2 Results

6.2.1 LED Heterostructures

Six GaAs/InGaP broad area LEDs, of varying material quality, will be compared with an AlGaAs based LED structure. The heterostructures are summarized in Figure 6.3. The InGaP based samples are essentially identical in structure, consisting of a 0.6 μm uninten-

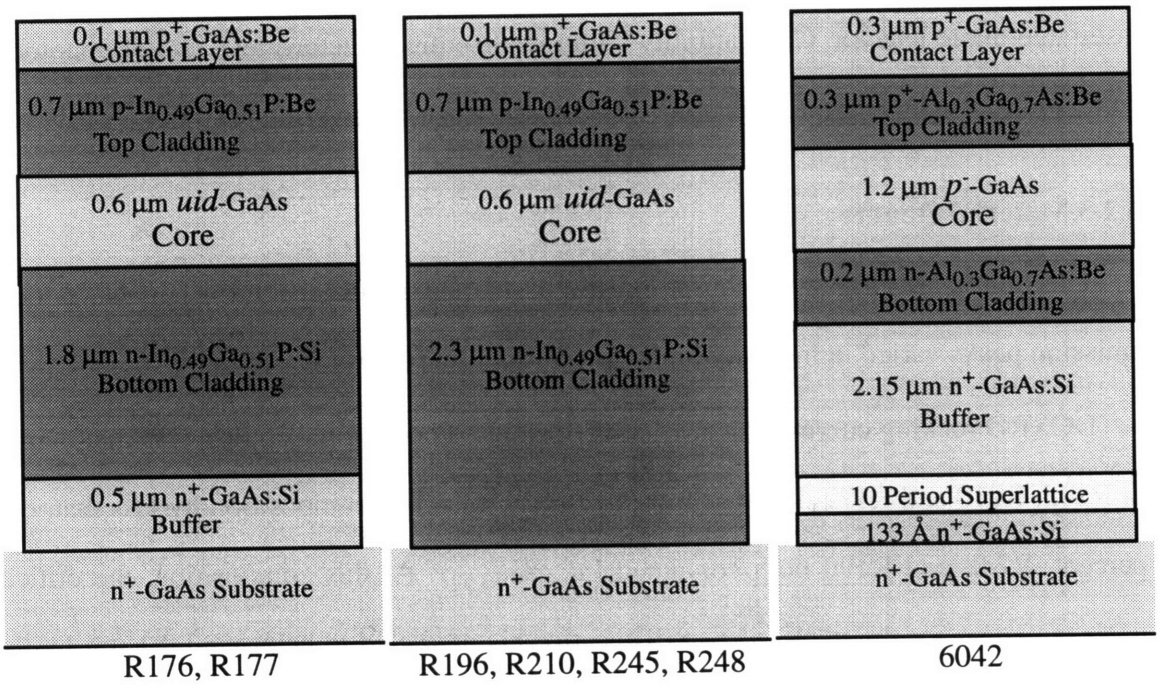


Figure 6.3: LED heterostructures of samples used for broad area LED study. Rnnn are InGaP based material grown by GSMBE. R196 was grown on a hydrogen plasma prepared substrate. 6042 is an AlGaAs based sample grown by solid source MBE [80]. The superlattice is 10 periods of 25 Å GaAs/ 25 Å $Al_{0.3}Ga_{0.7}As$.

tionally doped GaAs core between n- and p- doped InGaP claddings. All are grown on thermally desorbed surfaces, with the exception of R196. R196 was part of a hydrogen plasma oxide removal experiment. The primary difference in the AlGaAs based heterostructure is the 1.2 μm rather than 0.6 μm core layer thickness. However, similar AlGaAs based diodes with 0.6 μm cores have produced very similar results [81]. Also, the AlGaAs based structure uses a superlattice to block threading dislocations nucleated at the substrate surface [82].

6.2.2 LED Spectrum

A GaAs/InGaP DH device, R167, consisting of 0.2 μm of unintentionally doped GaAs clad by 1 μm n- and p- doped InGaP layers, and with a 0.1 μm p^+-GaAs contact layer was used for an electroluminescence measurement. The spectrum is shown in Figure 6.4. For

optical interconnect applications, the spectrum from the GaAs core must be detectable by a suitable photodetector. Compatibility with metal-semiconductor-metal (MSM) photodetectors fabricated using the standard Vitesse process has been verified [80].

6.2.3 Material Quality

The InGaP samples were chosen on the basis of their PL spectra. Their GaAs core emission peaks varied in intensity but were at or below 10 meV in width.

DCXRD rocking curves indicate that very good compositional control was maintained in R245. R210 and R177 deviated from the lattice-matched composition by less than one percent. R248 and R196 both contained $In_{0.48}Ga_{0.52}P$. At this composition, the critical layer thickness for the nucleation of dislocations is predicted to be around 0.1 μm by the force balance model [83,84] and around 20 μm according to the energy balance model [83,85]. It is not clear if the strain in these samples is affecting the material quality.

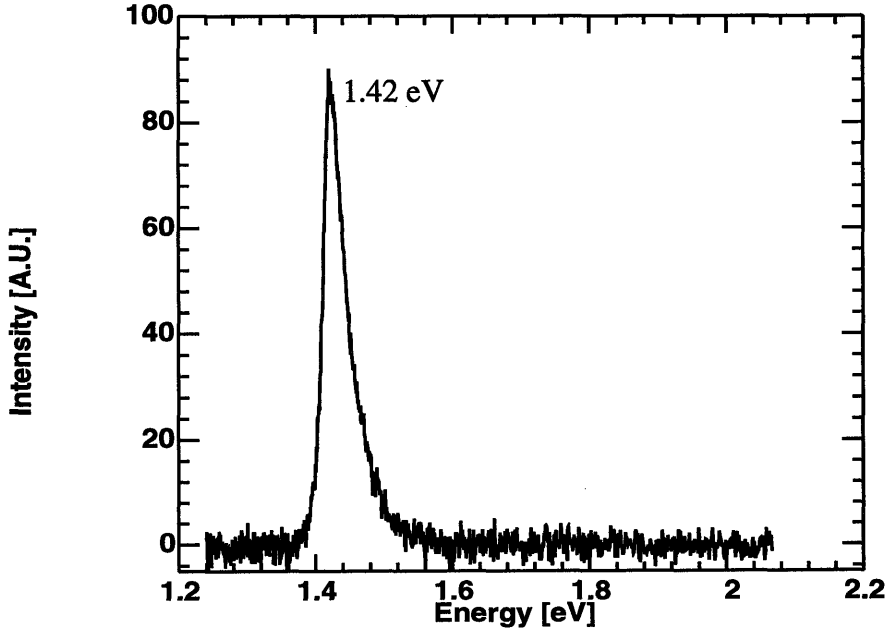


Figure 6.4: Electroluminescence spectrum of GaAs/InGaP DH device, R167. The spectrum is characteristic of the InGaP based LEDs.

Finally, the R176 DCXRD curve indicates poor material quality, including the presence of extra peaks.

It should be noted that timing problems during the computer controlled growth of R176 and R177 resulted in the growth of group III rich material and/or material of the wrong composition at the interfaces. This is thought to be manifest in the presence of oval-shaped defects densely dispersed across the epi surface. In R196, an attempt was made to mitigate this problem by increasing the growth interruption between the GaAs and InGaP layers as the group-V gases were being switched. This led to the observation of surface phosphorus displacement by arsenic during the interruption. The surface morphology of R196 included small round defects, but since this sample was involved in a hydrogen plasma oxide removal trial, the source of these defects is not entirely clear.

6.2.4 Current - Voltage Response

The current vs. voltage plot for the seven samples is shown in Figure 6.5. The turn-on voltage of the diodes is high due to large series resistances caused by poor metallization or low doping. The resistance also appears to be somewhat inconsistent among the different samples. This may be due to unequal lapping.

For the 500 μm diameter contacts, the current density at 0.1 A is 51 A/cm^2. By comparison, current densities injected into the processed AlGaAs are in the KA/cm^2 range for appreciable output power levels. Thus, the broad area LED measurement are being performed in a low current density regime. As discussed above, non-radiative current dominates the total diode current at very low current levels. In this regime, ln(I) is proportional to V/2kT. At sufficiently high currents where radiative recombination is dominant, the overall ln(I) curve is proportional to V/kT. Thus, a kink in the ln(I) vs. V curve identifies the current density needed overcome the non-radiative regime. The position of the kink is

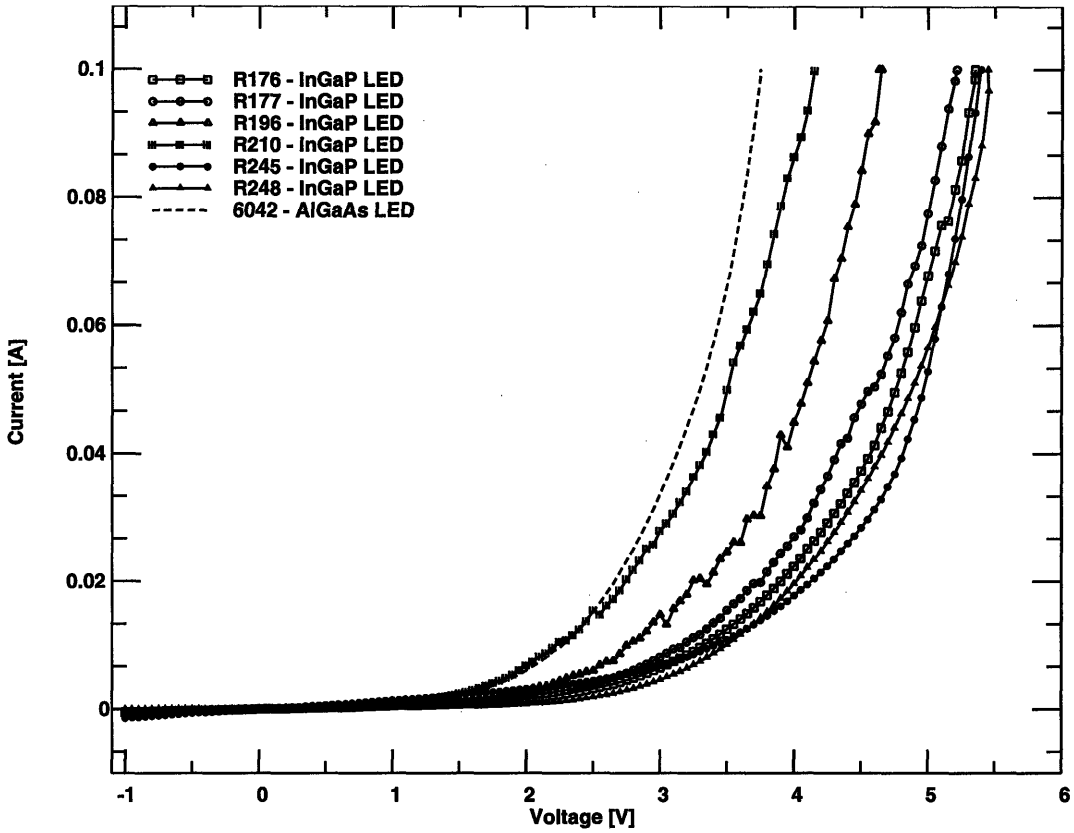


Figure 6.5: Current - Voltage response of the 500 μm diameter broad area LEDs tested. Large series resistances results in high turn on voltages.

indicative of the density of non-radiative recombination centers. A logarithmic I-V plot is shown in Figure 6.6. Indeed, kinks are visible, but the large and inconsistent series resistances, and significant heating, make accurate determination of meaningful kink points difficult.

6.2.5 Light Output - Current Response and Efficiency

The measurement setup used for the light-current response of the broad area LEDs is described in Appendix C. Figure 6.7 shows the light output power as a function of terminal current. The six InGaP based devices can be placed in three categories. R176 and R177 were of poor quality. Their commonality is the presence of poorly formed interfaces resulting from problems in the growth. R196 and R248 performed well, but only about half as efficiently as R210 and R245. The DCXRD curves of R196 and R248 both indicate

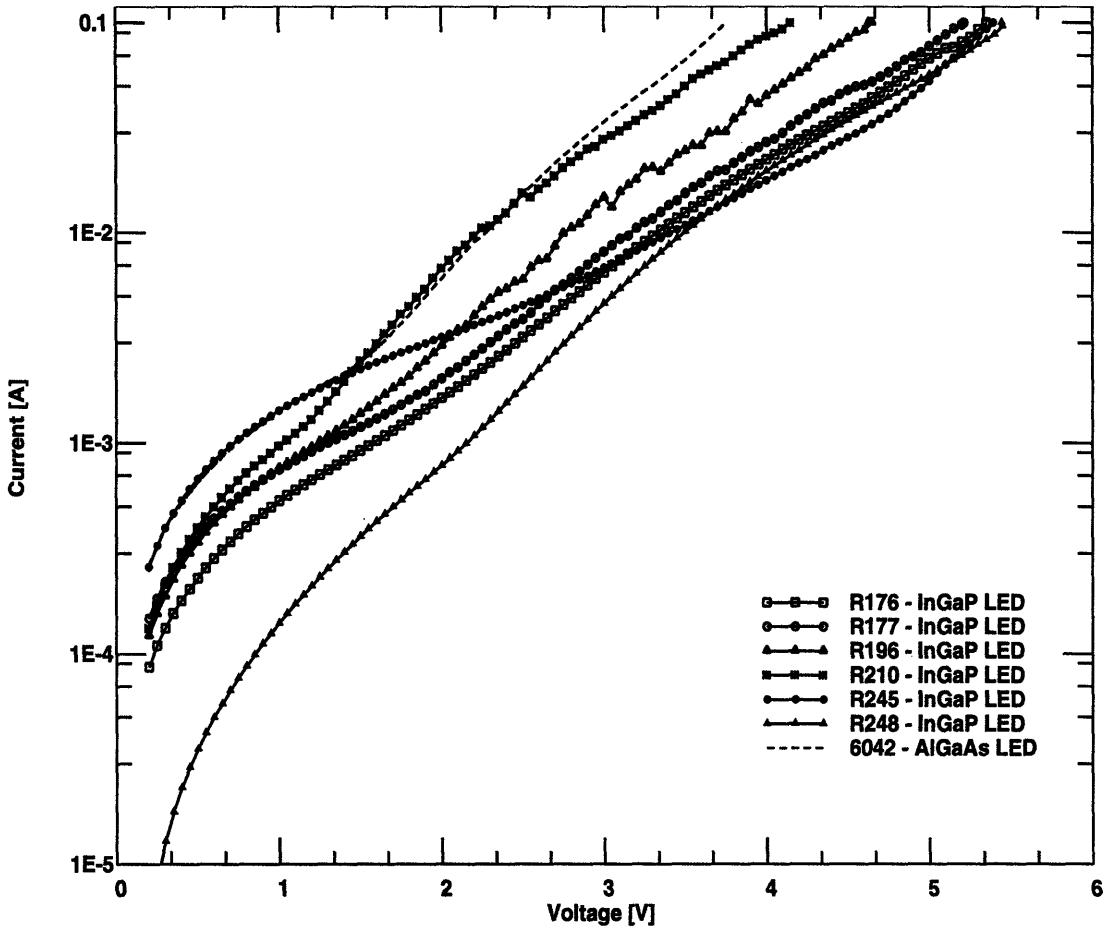


Figure 6.6: Logarithmic I-V curve for the broad area LEDs tested. A kink in these curves indicates the transition point from nonradiative to radiative dominated recombination. High, inconsistent series resistance, and significant heating makes the determination of kink points dubious.

that the InGaP composition was around $In_{0.48}Ga_{0.52}P$. R210 and R245 had InGaP within 1% of $In_{0.49}Ga_{0.51}P$ lattice-matched composition. Both of these samples emitted similarly large output powers. The AlGaAs based device, sample number 6042, had a similar response, though not as poor, as R177.

A more revealing description of LED performance is a plot of efficiency vs. logarithmic current, as shown in Figure 6.8. A summary of the efficiencies at 0.1 A input current, corresponding to 51 A/cm^2, is given in Table 6.2.

The grouping of R176 with R177, R194 with R248, and R210 with R245 is born out in the efficiency data. For currents below around 0.02 A (10 A/cm^2), R210 is the most effi-

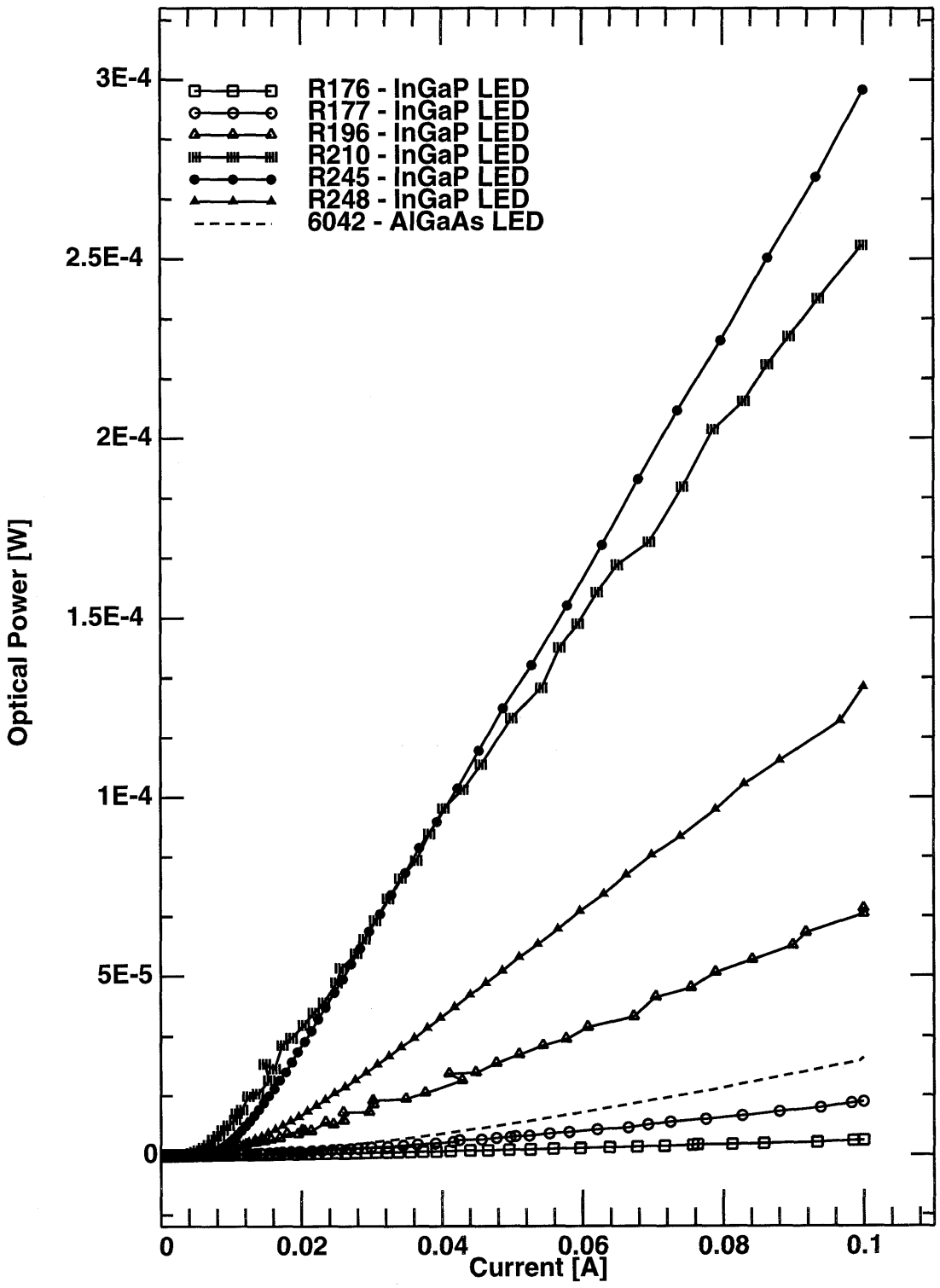


Figure 6.7: Light output power vs. current for the broad are LEDs tested. The curves are superlinear at very low currents, and become linear as the radiative recombination current component dominates.

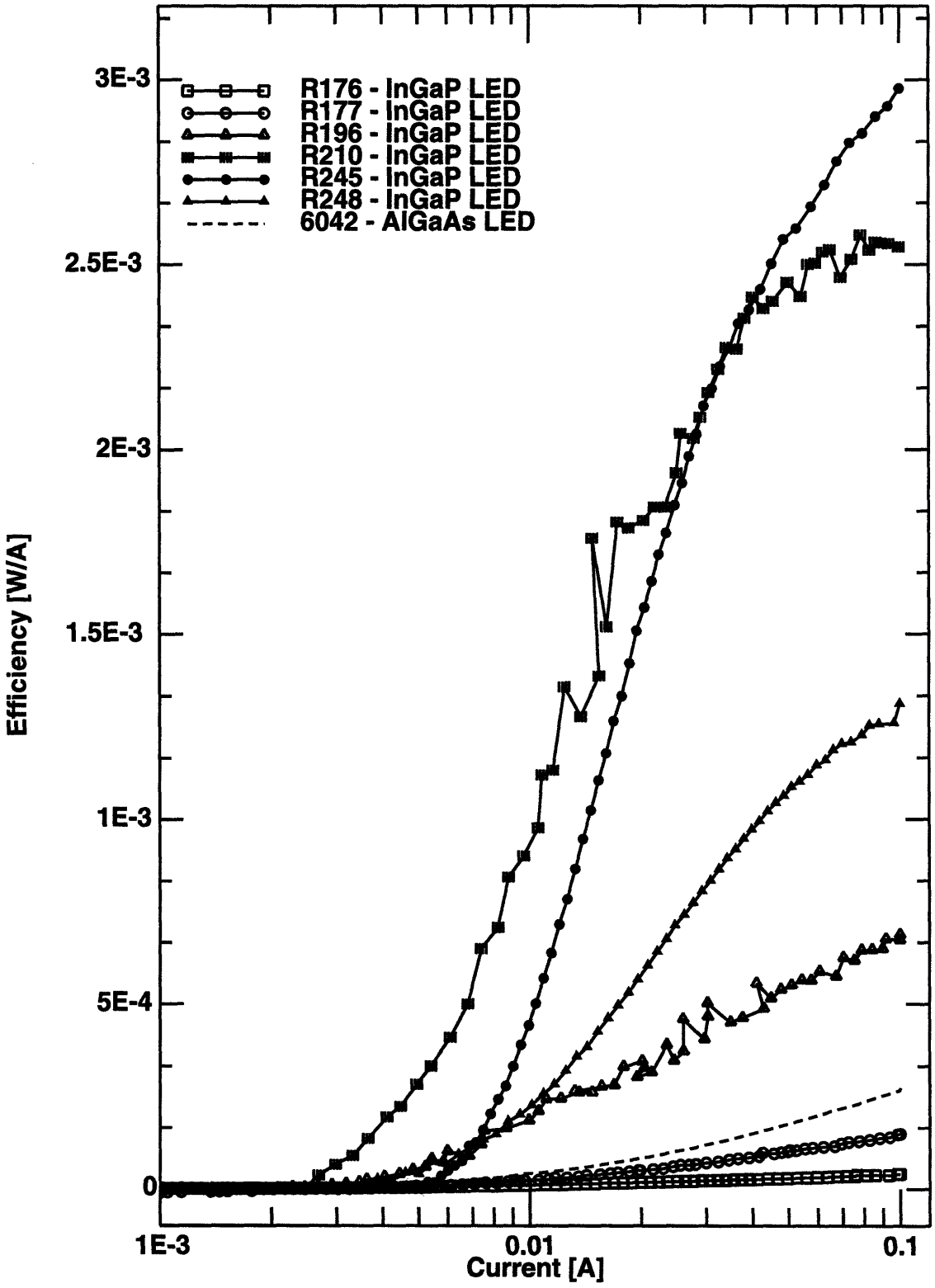


Figure 6.8: Efficiency vs. logarithmic current for the broad area LEDs tested.

	Efficiency $x10^{-3}$ [W/A]
R176	0.04
R177	0.2
R196	0.7
R248	1.3
R210	2.5
R245	3.0
6042	0.3

Table 6.2: Broad area LED efficiencies at 0.1 A drive current.

cient device, while above this current R245 is somewhat more efficient. The source of this disparity is unclear. The similarity between R196 and R248 is also very good at the lower currents, but above 0.01 A (5 A/cm^2) the efficiency of R248 begins to increase more rapidly.

R196, R210, R245, and R248 have qualitatively similar efficiency curves. In all four cases, the curve is superlinear at low current levels, then becomes linear, and eventually tends to saturate. R176 and R177, as well as the AlGaAs based 6042 share a different response. In the current range examined, the efficiency simply rises superlinearly. Comparison with Figure 6.2 shows that the same type of efficiency curve is observed for the fully processed LEDs.

6.3 Discussion

The most unambiguous conclusion that can be drawn is that at an injection current density of around 50 A/cm^2, a GaAs/InGaP LED can be up to a factor of ten more efficient than the EoE-compatible GaAs/AlGaAs LED used for comparison. If a similar improvement

applies to fully processed LEDs, then much less current will need to be injected to achieve the required light output, making such LEDs a valuable light source for optical interconnect applications.

The high interface recombination velocity for low temperature grown GaAs/AlGaAs interfaces is presumably the cause of the reduced efficiency of the AlGaAs based devices. The similarity in the efficiency curves of the AlGaAs sample with R177 is consistent with the suspected poor quality of the GaAs/InGaP interfaces in this sample. Furthermore, the dissimilarity of the efficiency curves of the more efficient InGaP based devices tends to confirm the formation of GaAs/InGaP interfaces with low interface recombination velocities.

With regard to the medium efficiency devices, R196 and R248, it can be noted that R245 and R248 were nearly identical with the exception of the slight composition error in R248. It is not clear how a deviation in composition of this magnitude affects efficiency. Also, R248 was grown using 0.4 μm/hr InP and GaAs growth rates as opposed to 0.5 μm/hr used for R245. This would increase impurity incorporation, but the magnitude of this effect is not known. R196 had roughly the same composition as R248, and was grown at the same, lower growth rate. The lower efficiency of R196 is probably due to the imperfect hydrogen plasma surface preparation procedure. Nonetheless, it is clear that the hydrogen plasma oxide removal technique is compatible with the growth of high quality LEDs.

As a final note, the extraction efficiency factor of d/l in (6.1) does not give a direct conversion between the broad area and fully processed results. At 50 A/cm^2, the AlGaAs based broad area LED has around the same efficiency as the most efficient fully processed LED does at nearly 10 KA/cm^2. It may be that at such high current densities, the assumption that d remains constant as l is scaled may break down due to current crowding. An

increase in d results in an even greater efficiency improvement as l is reduced, but a larger d also forces current near the etched mesa walls of the processed LED. If this were the case, surface recombination would play an important role in the efficiency reduction. Also, the presence of a dielectric layer over part of the processed LED surface may act as an antireflection coating, resulting in reduced light extraction.

Chapter 7

Laser Diodes

7.1 Introduction

Laser diodes used in a densely integrated OEIC must operate with minimal power consumption. Above threshold, laser diodes are very efficient, but power must be dissipated in order to reach threshold. Therefore, reduction of the laser threshold current is of primary importance in OEIC applications. As seen in Section 2.4, the reduction of J_{th} runs counter to the development of high power lasers used for pumping EDFA. In fact, for low power operation, a single quantum well separate confinement heterostructure (QW-SCH) may prove to be optimal.

The heterostructure used in this work is shown in Figure 7.1. It is based on the struc-

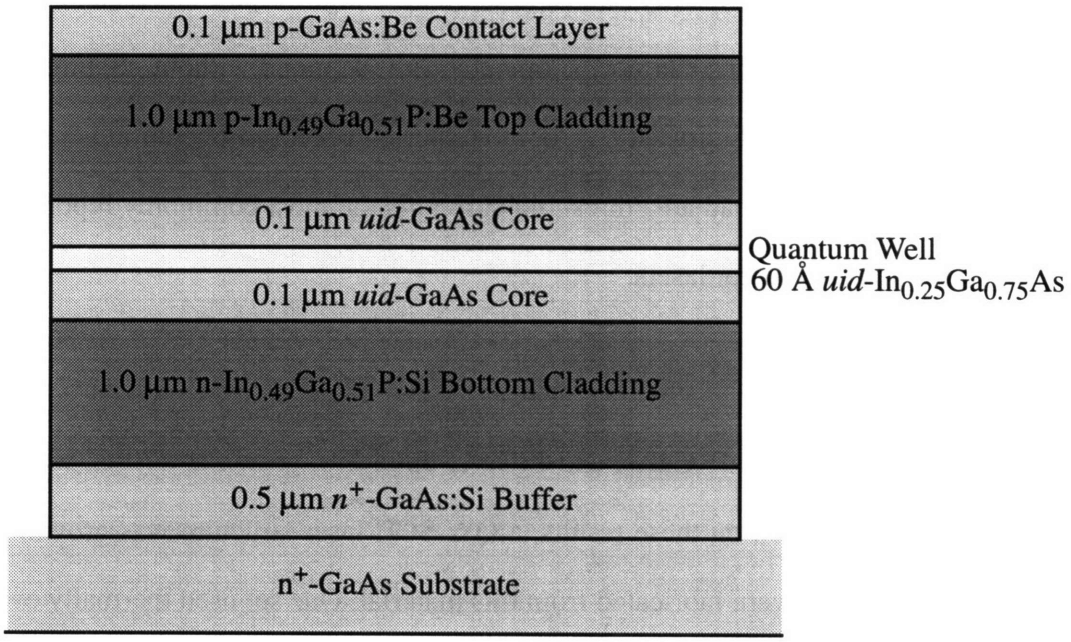


Figure 7.1: Strained InGaAs/GaAs/InGaP single quantum well separate confinement heterostructure (QW-SCH) used in this work.

ture used by Zhang, *et al.*, to achieve the very low threshold current density of 72 A/cm^2

[38,39]. In that work, the InGaP and InGaAs were grown at a substrate temperature of 500°C and the unintentionally doped GaAs was grown at 590°C. Following growth, the sample was rapid thermal annealed at 900°C for 1 sec. to improve the quality of the InGaAs quantum well. For EoE applications, the entire structure must be grown at or below 470°C. The purpose of the present chapter is to demonstrate that high quality laser diodes, as characterized by threshold current density, can be grown at this reduced substrate temperature.

The operating principles of semiconductor laser diodes are described in Appendix B. The broad area laser is, essentially, an implementation of a 2-D idealization. By using a very broad stripe to inject carriers, almost all processing related dependences are removed. Device performance depends only on material and facet quality. By using long optical cavity lengths (usually close to 1 mm), the facet loss, prorated over cavity length, is small in comparison to the material quality related loss. Since a large stripe area results in a large terminal current, these devices can not be operated in CW mode without cooling due to the large amount of power dissipated. At room temperature, pulsed operation is required. Pulsed room temperature broad area threshold current is the most commonly reported figure of merit for semiconductor lasers.

7.2 Results

The material quality of InGaP, GaAs, and InGaAs epilayers, grown at 470°C, were discussed in Chapter 5. Based on these results, a QW-SCH laser structure was grown. Two sets of broad area lasers were fabricated from this material. One set used thermally evaporated Cr/Au as the ohmic contact to the p-type GaAs contact layer. A 98 μm wide stripe was defined using standard lift-off techniques. On the second set, Ti/Au was sputtered on the p-type GaAs, and the stripes were defined using a wet etch. The Au was etched using a

bromine based gold etchant, which does not etch Ti. The Ti was then etched in BOE. Since the injected current must pass through the 1 μm top cladding layer before reaching the active region, by assuming isotropic current spreading the lateral current spread may be approximated as 1 μm on each side of the stripe. Thus, the 98 μm stripe yields a 100 μm wide current injection region.

7.2.1 Laser Material Results

The laser material was characterized using double crystal x-ray diffraction (DCXRD), photoluminescence (PL), and electroluminescence (EL).

A DCXRD curve for the strained InGaAs/GaAs/InGaP QW-SCH is shown in Figure 7.2. The precise compositional control needed to maintain tight lattice matching of the

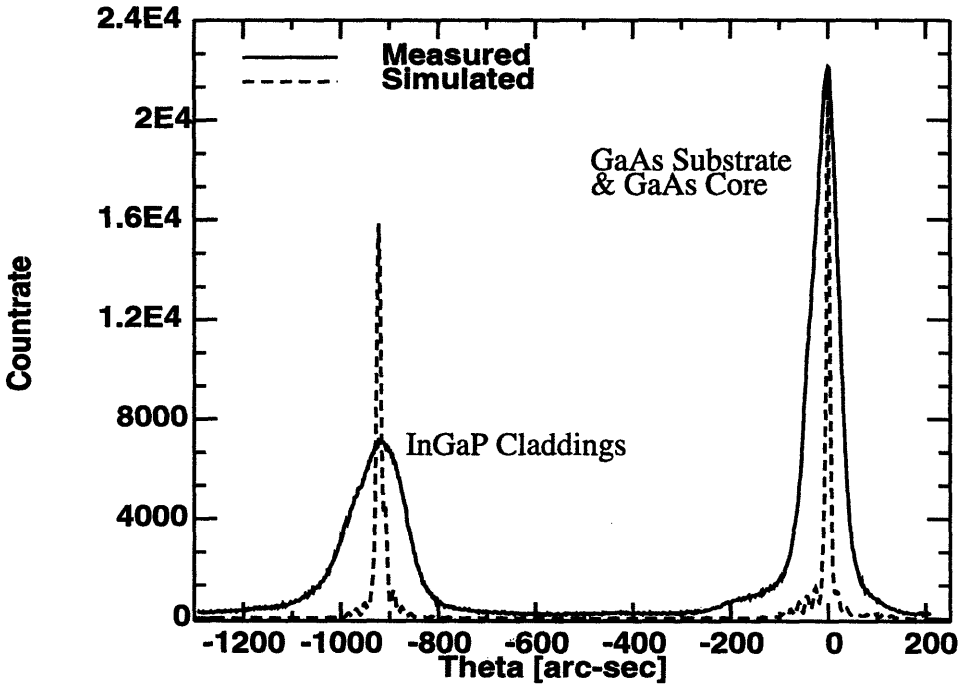


Figure 7.2: DCXRD for the strained InGaAs/GaAs/InGaP QW-SCH laser heterostructure studied. The InGaP peak is just over 900 arc-sec to the compressive side of GaAs. The DCXRD simulation corresponds to 53.3% In composition, as opposed to the target value of 49%.

InGaP to the GaAs substrate was not achieved in this sample. The In composition was 53.3% rather than the target value of 49% for lattice-matched InGaP. This resulted in the presence of non-negligible strain in the material, as seen in the roughly 900 arc-sec separation between the GaAs and InGaP peaks. The theoretical critical layer thickness for InGaP at this composition is predicted by the force balance model to be less than 0.1 μm [83,84], and by the energy balance model to be around 2 μm [83,85]. The latter estimate is consistent with experimental work on strained InGaP epilayers [83]. Total InGaP thickness in the laser structure is 2 μm, raising the possibility of strain induced dislocations. The manifestation of these defects on device characteristics remains to be seen.

PL results for the laser material are shown in Figure 7.3. The high In composition reduced the InGaP bandgap. For lattice-matched InGaP, the low temperature PL peak

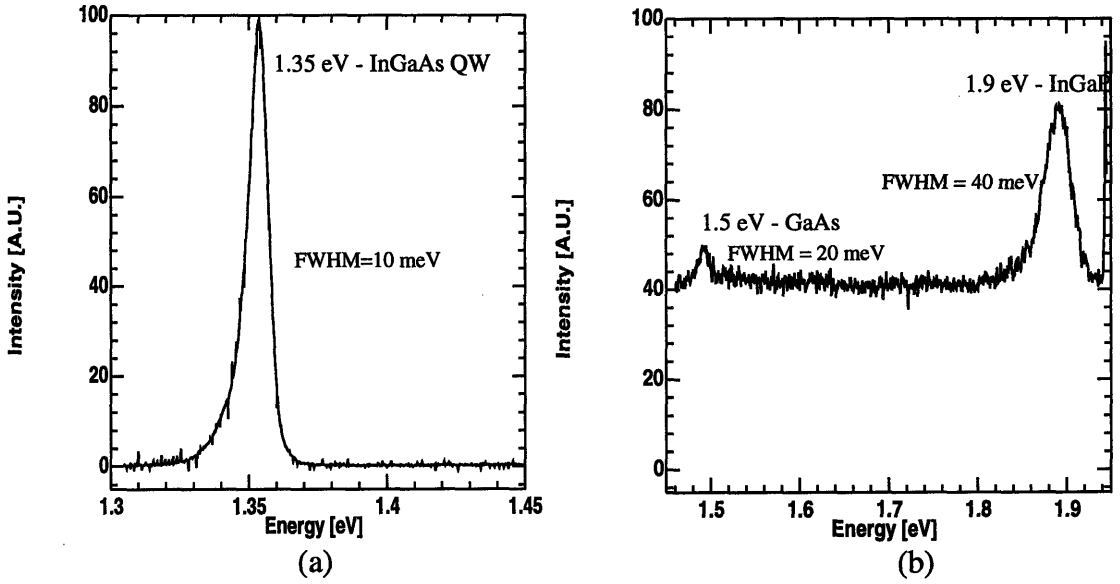


Figure 7.3: 10 K PL of strained InGaAs/GaAs/InGaP QW-SCH laser heterostructure. (a) shows strong emission and narrow line width from the quantum well. (b) shows emission from the GaAs core and doped InGaP claddings. The position of the InGaP peak is below the nominal value of 2 eV for lattice matched InGaP, in agreement with DCXRD results indicating excess In composition. A He:Ne pump laser was used in the measurement, and is visible at the far right of the spectrum in (b).

occurs at 2 eV and would not be excited by a 1.959 eV He:Ne pump laser, but a peak corresponding to the narrower bandgap of $In_{0.53}Ga_{0.47}P$ is seen in this PL scan. The FWHM of the InGaP peak is around 40 meV. Bulk epitaxial GaAs PL from a GaAs/InGaP double heterostructure has been measured with a FWHM of 5 meV under identical measurement conditions, and $In_{0.5}Ga_{0.5}P$ (sample R83) was previously found to have a PL peak FWHM of 8.8 meV [77]. The significantly broader peak may be indicative of the presence of strain induced defects. The GaAs peak is at the expected value of 1.5 eV, but has a FWHM of 20 meV. Clearly, the optical quality of this material is less than optimal. The quantum well produces a strong PL peak at 1.35 eV. The FWHM of the quantum well peak is 10 meV. For high quality InGaAs quantum well samples, peak width of around 4 meV are expected [86]. The FWHM of the present sample is roughly twice as wide, neglecting possible differences in PL measurement resolution. Apparently, dislocations initiated in the InGaP have not overwhelmingly degraded the optical quality of the InGaAs quantum well.

To study the quality of the InGaAs emission under electrical excitation, and to confirm the operating wavelength of the laser, an EL spectrum was determined. Figure 7.4 is the EL emission spectrum of the laser heterostructure. Light was produced at 0.99 μm, close to the target value of 0.98 μm. The FWHM of the emission peak is around 50 meV, consistent with thermal broadening.

DCXRD and PL results indicate that the InGaP cladding layers are not of optimal quality due to poor lattice match. However, PL shows a reasonably narrow emission peak from the quantum well; good laser performance may still be possible. EL confirms a correct emission wavelength.

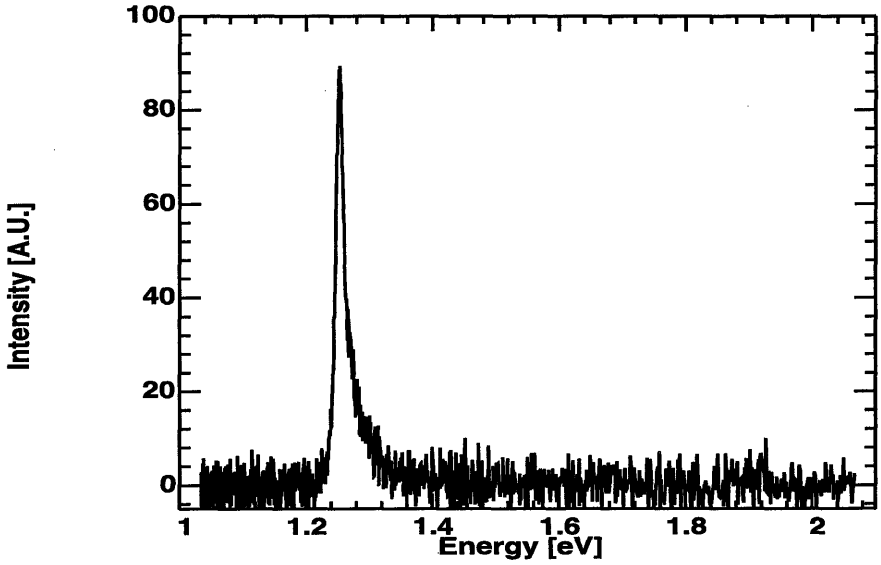


Figure 7.4: 300 K EL of strained InGaAs/GaAs/InGaP QW-SCH. The FWHM is around 50 meV, consistent with thermal broadening. The peak in energy at 1.25 eV corresponds to emission at 0.99 μm, rather than the target value of 0.98 μm.

7.2.2 Laser Results

The pulsed mode laser characterization setup is described in Appendix C. The optical power is believed to be underestimated by a factor or 2 to 3. This factor is not taken into account in any value quoted here.

Figure 7.5 is a plot of light output versus pulsed current density for a number of broad area devices fabricated from the strained InGaAs/GaAs/InGaP QW-SCH material. Among the devices tested, the lowest pulsed room temperature threshold current density was 200 A/cm^2. It was obtained from a 792 μm long device with Cr/Au ohmic contact metal. From a 284 μm device with Ti/Au ohmic contact stripe, 80 mW of output power per facet was measured (not including the correction factor). This device did not fail during the test. Devices with the same metallization and length produced consistent results.

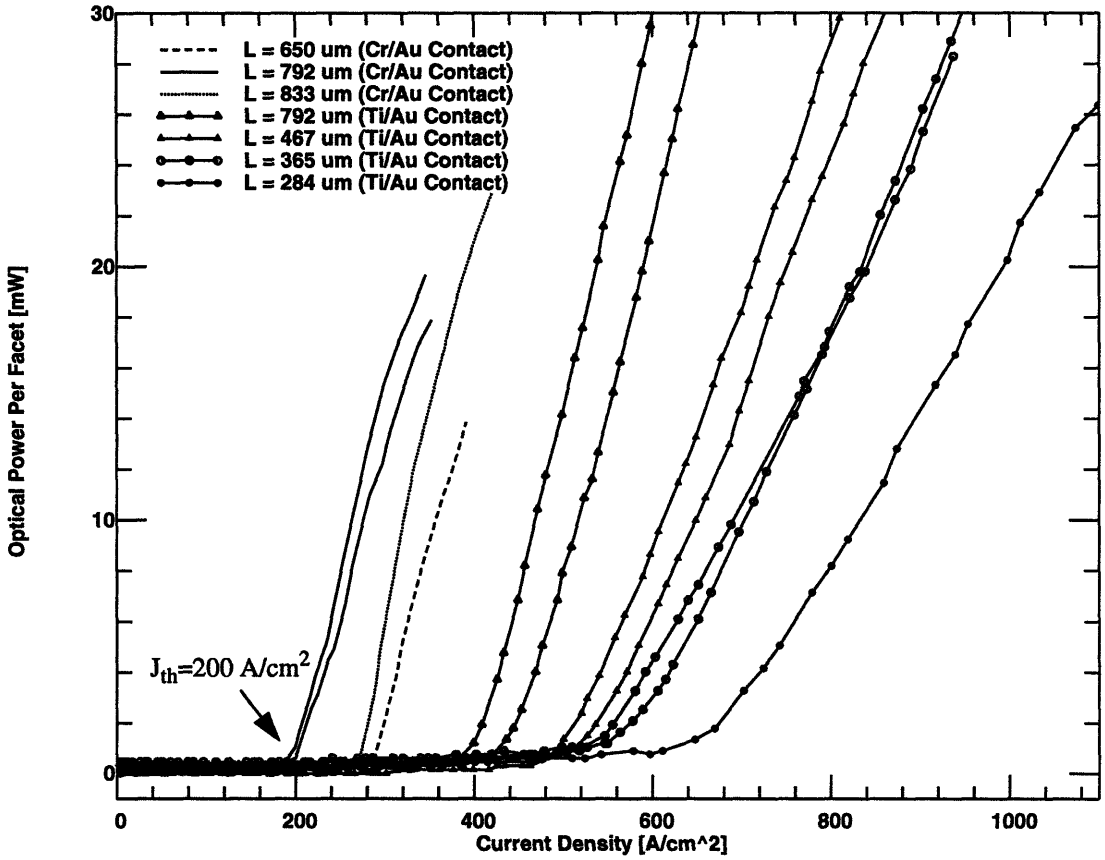


Figure 7.5: Pulsed room temperature light output power vs. input current density for strained InGaAs/GaAs/InGaP QW-SCH broad area lasers. Ohmic contact stripes were made with non-annealed Cr/Au or Ti/Au metallization. Cavities of various lengths were tested. A low threshold current density of 200 A/cm^2 was attained with a 792 μm long Cr/Au contacted device. A 284 μm Ti/Au contacted device output over 80 mW without failure.

As expected theoretically, the threshold current density diminishes with increasing cavity length. However, a factor of two difference is seen in the threshold current density between the Cr/Au and Ti/Au 792 μm devices. This level of threshold current fluctuation is not uncommon for non-annealed ohmic contacts [86]. Although they had higher threshold currents, the Ti/Au contacted devices were much more robust, achieving much higher output powers than the Cr/Au contacted devices. This is attributed to the superior adhesion of Ti and the greater thickness of Au in the Ti/Au scheme. The latter feature allows

more uniform current injection since the less resistive stripe metal provides better current spreading.

7.3 Discussion

The 200 A/cm^2 threshold current density is less that a factor of three above the 72 A/cm^2 reported by Zhang, *et. at.* [38,39]. This shows that state of the art laser diodes can be fabricated under EoE compatible growth conditions.

The material used in this study was of reduced quality due to inaccurate InGaP composition. As shown in Chapter 5, higher quality material may be produced without any change in growth conditions aside from the InGaP composition. Further investigation of InGaP based lasers for EoE integration must begin with the growth of higher quality laser material.

Aside from the inadvertent degradation of material quality, the performance of the devices tested may have been sacrificed because the growth parameters used in this study were not optimized to reduce threshold current. While the substrate temperature is dictated by the constraints of the EoE thermal budget, optimization of the heterostructure, growth rates, and group V overpressures may improve the laser's performance.

By comparison with the 200 A/cm^2 threshold current obtained in this work, the AlGaAs based laser optimized by Shenoy, *et. al.*, for growth at 530°C by conventional MBE techniques had a threshold current density of 1800 A/cm^2 [5]. Using unconventional, reduced overpressure growth, a threshold current density of 600 A/cm^2 has been reported [15,16]. InGaP based laser diodes grown by conventional MBE techniques are, thus, a very attractive choice for use as EoE compatible optical emitters.

Chapter 8

Conclusion

8.1 Summary

The epitaxy-on-electronics (EoE) integration scheme has been previously used to successfully fabricate optoelectronic very large scale integration (OE-VLSI) circuits using AlGaAs based LEDs and lasers. In EoE integration, device material is epitaxially grown in foundry opened windows in the dielectric stack of fully processed VLSI GaAs MESFET circuits. The ICs used in this work were commercially fabricated by Vitesse Semiconductor, Inc. The reliability of EoE integration and the performance of the optoelectronic integrated circuits (OEICs) produced has been hindered by three issues: dielectric growth window (DGW) preparation, GaAs native oxide removal, and compromised performance of EoE compatible grown AlGaAs based devices. The present work refines the EoE integration technology by addressing these three issues.

8.1.1 Dielectric Growth Window (DGW) Preparation

The original procedure for DGW preparation used a foundry CF_4/O_2 reactive ion etch (RIE) of the dielectric stack to expose the GaAs substrate. This procedure left residues, consisting of SiO_2, Si_3N_4, and fluorinated hydrocarbons, in contact with the substrate. These residues must be removed before growth. The DGWs were cleaned by additional, gentle CF_4/O_2 RIE etching followed by wet etching in buffered hydrofluoric acid (BOE). The AlGaAs based device material grown in these DGWs had slightly degraded surface morphology, as compared to material grown simultaneously on a bulk GaAs wafer, but produced identical device characteristics.

Approximately one year after the successful application of the above DGW preparation method, the same procedure was used to ready ICs for the growth of InGaP based emitters. All of the residue could not be removed with CF_4/O_2 and BOE. Using BOE and several hours of O_2 plasma exposure the residues were removed, but the underlying GaAs was seen to be roughened. The cause of the substrate roughening and the failure of the old preparation method is hypothesized to be gradual etching of the GaAs by the fluorinated hydrocarbons. InGaP based LED material grown in these DGWs had very rough morphology.

A new DGW preparation technique has been developed. The foundry RIE etch is stopped short of the GaAs substrate, preventing contact of the residue with the GaAs. The remaining dielectric is then etched with BOE. Using this procedure, DGWs have been prepared with no visible morphology, and material grown in these DGWs has identical morphology as material grown simultaneously on bulk GaAs.

8.1.2 Low Temperature GaAs Native Oxide Removal

Vitesse GaAs MESFET circuits degrade in performance when exposed to temperatures above 470°C. In conventional MBE practice, the GaAs native oxide is removed prior to growth nucleation by briefly elevating the sample to 580°C. This oxide removal process degrades the electronics. A low temperature GaAs native oxide removal process was investigated in order to eliminate electronic device degradation. This new oxide removal process uses atomic hydrogen, in a H_2/Ar fed RF plasma, at substrate temperatures around 300°C. This thesis shows that high quality material can be grown after low temperature oxide removal using atomic hydrogen.

8.1.3 EoE Compatible Growth of Light Emitters

InGaP based LED material, grown entirely at 470°C, was compared with a similar structure based on AlGaAs using broad area structures. The efficiency of the best GaAs/InGaP LEDs was roughly a factor of ten better than the GaAs/AlGaAs LED material tested.

A strained InGaAs/GaAs/InGaP quantum well separate confinement heterostructure (QW-SCH) was grown and processed into broad area lasers. A low threshold current density of 200 A/cm^2 was measured. Grown entirely at 470°C, these devices performed comparably to similar devices grown under optimized conditions, and represent a significant improvement over AlGaAs based laser diodes grown at 530°C.

8.2 Further Investigation

There are two primary areas for further investigation: low temperature oxide removal and the integration of high performance light emitters.

Low temperature oxide removal is at an early stage of its development, both within this research group and throughout the MBE community. A procedure to completely and with repeatability remove all surface oxide without damaging the GaAs substrate must be developed. Because it is potentially more gentle to the substrate, thermally cracked H_2 may prove to be more compatible with subsequent growth than the hydrogen plasma source used in the present work.

The integration of the LEDs and laser diodes developed in this thesis into functional OEICs is an immediate research objective. Further refinement of these devices, and the development of more advanced devices should follow. In particular, vertical cavity surface emitting lasers (VCSELs) are recognized as excellent light sources for optical interconnect applications due to their narrow, circular emission patterns and low threshold cur-

rents. A small footprint and inherent vertical emission eases the integration of VCSEL as compared to in-plane lasers. The availability of an integrated VCSEL will open important optoelectronic systems applications to EoE integration.

Appendix A

Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is a technique used to grow semiconductor crystals. At its core, a MBE system is similar to a simple thermal evaporator, as may be used for metal deposition. In an evaporator, a sample is placed in line-of-sight of "boats" containing the source material. With the chamber background pressure in the high vacuum regime (10^{-6} Torr range), the boats are heated in order to desorb material from the sources. The desorbed material propagates to the target where is adheres, forming a thin film.

MBE differs from thermal evaporation in two fundamental ways: 1) the use of an ultrahigh vacuum environment, and 2) material is not deposited, but epitaxially grown.

A.1 The GSMBE System

The growths in this thesis were carried out in a Riber Instruments, SA, 32P gas source MBE (GSMBE) machine. GSMBE differs from solid source MBE in that the group-V sources are derived from the thermal cracking of arsine (AsH_3) and phosphine (PH_3). The solid source effusion cells are still used for the group-III and dopant elements.

The III-V GSMBE chamber is part of an integrated III-V/II-VI epitaxy system. As shown in Figure A.1 the second GSMBE chamber is equipped for the growth of II-VI compound semiconductors. The II-VI chamber also contains a hydrogen plasma source used in the low temperature oxide removal experiments of Chapter 4. A closer look at a GSMBE chamber is given in Figure A.2, where in addition to the effusion cells, the chamber also has a thermal cracker through which arsine and phosphine are injected.

A.2 Ultrahigh Vacuum Environment: Monolayer Control

Unlike thermal evaporation, which is carried out in a bell jar, MBE uses an ultrahigh vac-

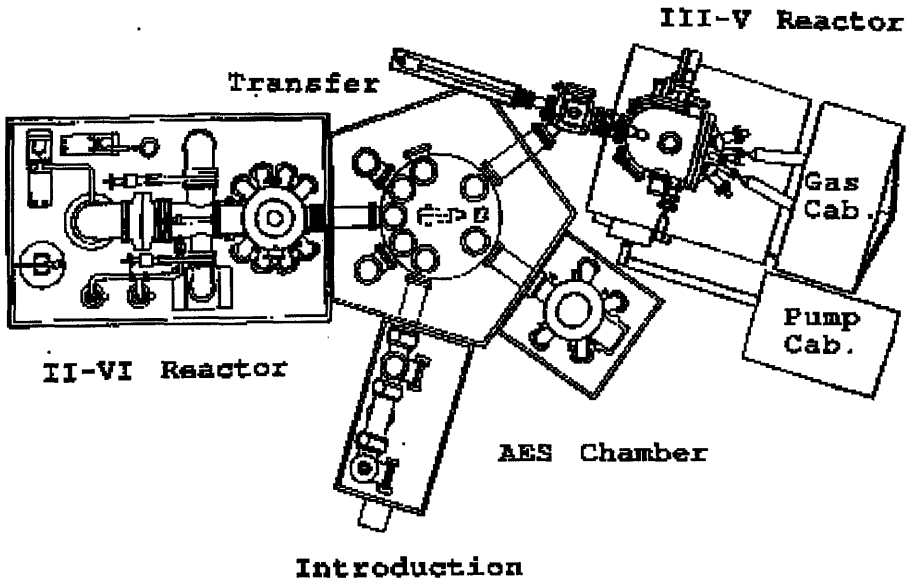


Figure A.1: The III-V GSMBE reactor used in this thesis is part of an integrated III-V/II-VI epitaxy system. The III-VI reactor is connected, *in situ.*, to another GSMBE chamber equipped to grow II-VI compound semiconductors. The II-VI chamber also contains the hydrogen plasma source used to investigate low temperature oxide removal. Figure A.2 details the III-V reactor.

uum (UHV) system. Base pressures (not during growth) are around 10^{-10} Torr. To maintain such low pressures, MBE chambers are outfitted with various pumps, including a liquid nitrogen cooled shroud inside the chamber. A tremendous amount of time and money must be exerted to outfit and maintain such a system.

What is the benefit of UHV? During growth, chamber pressures of around 10^{-6} Torr are experienced in GSMBE. At this pressure, the mean free path of a particle in the chamber is 30 m. Atoms are emitted from the sources with thermal velocities of 500 m/s. This means that the time of flight from a cell to the substrate, roughly 0.25 m away, is less than 1 msec. Now, typical growth rates in MBE are around 1 μm/hr, or around 1 monolayer/sec (ML/s). By placing a shutter, which can be opened or closed in around 0.1 sec., in front of the cells, growth can be controlled with monolayer precision [56].

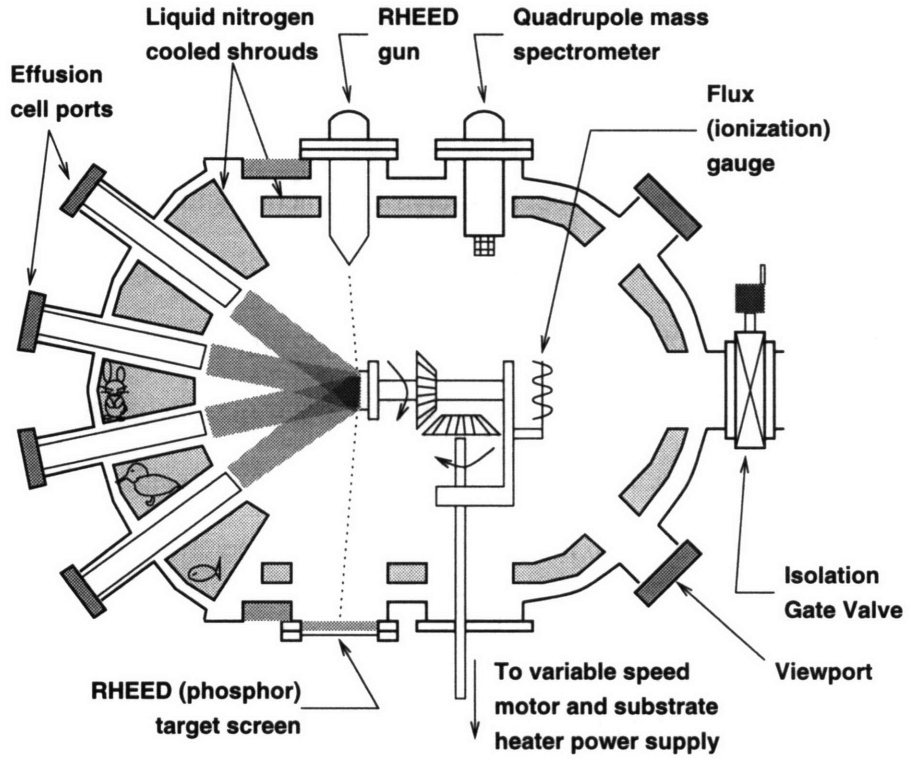


Figure A.2: Molecular beam epitaxy (MBE) chamber. Figure from [87].

The very low base pressures in MBE mean a very low concentration if impurities in the chamber. These impurities are incorporated into the growing crystal much slower that 1 μm/hr. If higher base pressures were used the impurity concentration would be higher. Also, the growth rates would have to be reduced in order to allow monolayer control. Material grown in this way would contain a high impurity concentration.

Thus, a UHV environment allows the growth of high purity compound semiconductors with control of layer thickness on the monolayer scale. The ability to control layer thicknesses with such precision is what allows the fabrication of sophisticated compound semiconductor devices such as quantum well laser diodes.

An additional advantage of operating in an UHV environment is that the growth surface can be monitored, *in situ*, using a diffraction pattern from a high energy electron

beam. This is referred to as reflection high energy electron diffraction (RHEED) and will be discussed below.

A.3 Crystal Growth

High performance semiconductor devices rely on semiconductors with long range order. In thermal evaporation, films simply adhere to the sample forming an amorphous film, which is not acceptable for most semiconductor device applications. In compound semiconductors, such as GaAs, there is the additional issue of stoichiometry. This section describes the growth mechanism for stoichiometric III-V compound semiconductors. The growth process can be broken up into the steps of beam generation, adsorption, and crystallization. These steps are discussed below.

A.3.1 Beam Generation: Beam Equivalent Pressure

Molecular beams of group-III elemental source material are produced by heated effusion cells. The flux of these species typically determines the growth rate, and is set by controlling the temperature of the effusion cell. Experimentally, the flux is characterized by placing an ionization gauge, a type of pressure meter, at the position of the substrate. The pressure produced at the substrate by species emitted from a cell is called the beam equivalent pressure (BEP). For growth rates of around 1 μm/hr, the BEP of In, Ga, and Al are all on the order of 10^{-7} Torr, as tabulated in Table A.1 [56].

In GSMBE, the group-V atoms are produced by thermally cracking arsine and phosphine. The flow rate of these gases is precisely controlled by a mass flow controllers. BEPs for As and P can not be determined, however, since they are accompanied by a large amount of hydrogen gas which was produced from the cracking.

	Cell Temperature [°C]	BEP $x10^{-7}$ [Torr]
In	750-900	1-5
Ga	950-1050	1-3
Al	1050-1150	1-5

Table A.1: Typical effusion cell operating temperatures and corresponding beam equivalent pressures [56].

A.3.2 Adsorption: Control of Stoichiometry

To achieve high material quality, the number of group-III and group-V atoms incorporated into the crystal must match within 10 ppb. This is referred to as stoichiometric growth. Group-III fluxes, however, can only be controlled to within 1% [56]. Under these circumstances, stoichiometric growth would be very difficult, if it were not for a beautiful twist of nature: by a judicious choice of the substrate temperature and source BEPs, a condition results in which all group-III elements arriving at the surface are adsorbed while group-V elements are adsorbed only to the point of exactly balancing the group-III elements present on the surface. In this case, the group-III elements are said to have a unity "sticking coefficient" while the group-V elements have sticking coefficients much less than one.

What is the origin of the sticking coefficients of the group-III and group-V elements? Consider, for example, liquid Ga on an inert substrate in thermal equilibrium with its environment. At a given temperature there exists a certain partial pressure of Ga vapor over the liquid Ga. This pressure is called the "vapor pressure", and is required to maintain a balance between adsorption and desorption of Ga from the liquid. If the partial pressure of Ga vapor is below the vapor pressure, Ga will desorb from the surface in an attempt to

achieve thermal equilibrium. If, by external means, the partial pressure of Ga vapor over the liquid Ga is increase above the vapor pressure, Ga will adsorb onto the surface. In GSMBE, the partial pressures of the group-III constituents are related to the BEP, and the partial pressure of group-V constituents is linked to the gas flow rate.

The vapor pressures of the group-III elements Ga, In and Al, the group-V elements As and P, and the dopant Si are plotted versus temperature in Figure A.3. The vapor pressures

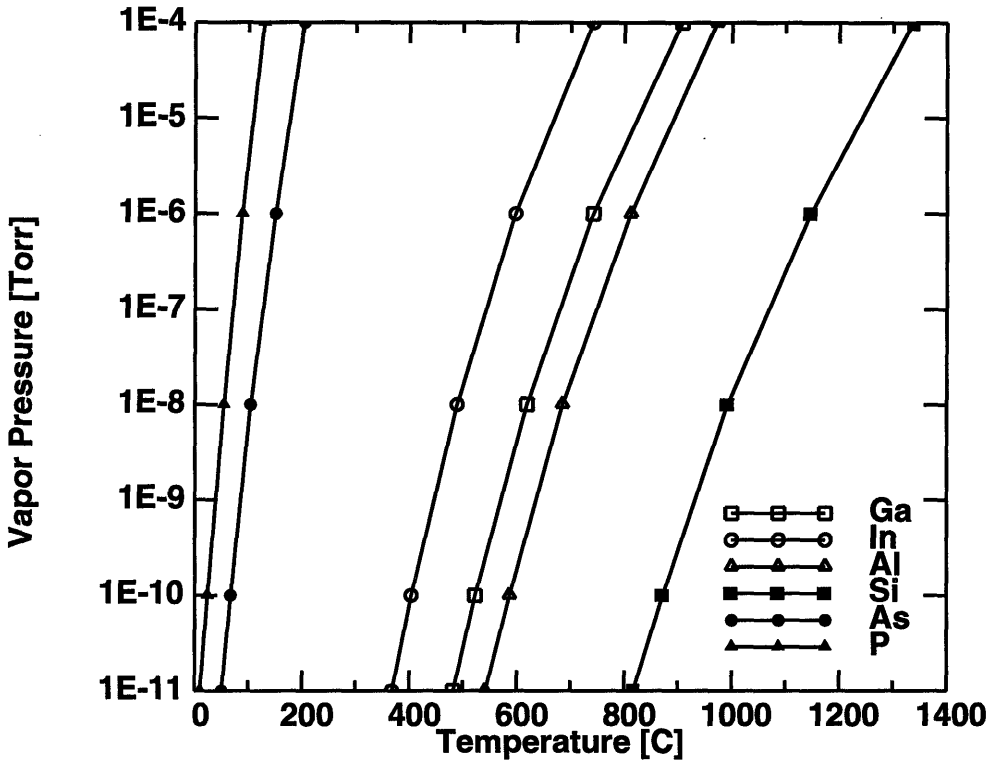


Figure A.3: Vapor pressure as a function of temperature for group-III (Ga, In, Al), and group-V (As, P) elements used in some III-V compound semiconductors. Also shown is the data for the group-IV element Si, which is an n-type dopant in III-V semiconductors.

of the group-V elements, As and P, are seen to be many orders of magnitude greater than the group-III elements. This fortuitous discrepancy allows for the growth of stoichiometric III-V compound semiconductors. Consider the growth of GaAs at a substrate temperature of 600°C. As seen in Table A.1, the BEP of Ga is around 10^{-7} Torr for reasonable growth

rates. The equilibrium vapor pressure over the substrate at 600°C is, according to Figure A.3, is around 10^{-8} Torr. Because the partial pressure of the Ga vapor, which is set by the BEP, is an order of magnitude greater than the equilibrium vapor pressure, Ga must adsorb to the surface. In fact, nearly all of the Ga arriving at the surface is adsorbed, thus the unity sticking coefficient value. The adsorption of Ga is said to be "arrival rate limited".

Arsenic, however, has a vapor pressure at 600°C that is many orders of magnitude greater that the available As partial pressure. The As partial pressure required to force adsorption of As exceed even the GSMBE total chamber pressure of around 10^{-6} Torr during growth. There is no way, at such pressures and temperatures, to maintain an adequately high partial pressure of As to force adsorption. In fact, As on the surface will readily desorb. Of course, As must adsorb if a crystal is to be grown. The mechanism is not thermodynamic, however, but chemical. While elemental As is not stable on the surface due to its high vapor pressure, GaAs *is* stable for substrate temperatures below the GaAs congruent sublimation temperature of 580°C-600°C [56]. Arsenic will bond with Ga on the surface of the substrate to form GaAs. Thus, only as much As is adsorbed as there is Ga on the surface, and perfect stoichiometry is maintained.

A.3.3 Crystallization: Surface Mobility

As stated above, group-III elements adsorb to the substrate due to their low vapor pressure while group-V elements only adsorb as a result of crystal formation. The adsorbed group-III atoms are referred to as adatoms. Adatoms migrate on the substrate surface due to thermal motion. Through their random motion, the adatoms "feel" the underlying crystal surface and find low energy minima corresponding to group-III lattice sites. Since an ample supply of group-V species is present above the surface, a III-V pair incorporates into the crystal when the adatom finds a suitable lattice site.

A monolayer is one half of a unit cell, and consists of a group-III and a group-V layer. Monolayer growth proceeds through the formation of monolayer islands. New adatoms migrate on the surface until they come to rest at the edge of an island. The islands grow in area until they coalesce and completely cover the growth surface.

The surface mobility of adatoms is an important factor in determining material quality. To maintain ideal, 2-D growth, the surface diffusion length of the adatoms must be greater than the distance to an island edge, otherwise multiple-monolayer variations will exist across the surface (3-D growth). For a given group-III species, the surface mobility is affected by the substrate temperature and the group-V overpressure. Increasing the substrate temperature increases adatom mobility by providing more thermal energy. Increasing group-V overpressure decreases adatom mobility by providing more frequent opportunities for group-III/group-V interaction.

When the growth rate is slow enough, that is when the surface diffusion length greatly exceeds the average distance between islands, adatoms fill in essentially all lattice sites on the surface before a new monolayer is initiated. Thus, an atomically smooth surface is achieved at the end of each monolayer of growth. This is termed 2-D growth. As the growth rate is increased, the diffusion length decreases such that the group-III/group-V pairs are incorporated into the crystal before an atomically smooth surface is formed. In a sense, several monolayers are grown simultaneously. This is known as 3-D growth as the growing surface is rough.

A.4 Reflection High Energy Electron Diffraction (RHEED)

A.4.1 In Situ Surface Characterization

As shown in Figure A.2, a RHEED gun accelerates electrons to 10 KeV and focuses a beam onto the substrate at an oblique angle. The electron beam is diffracted from the sur-

face and forms an image on a phosphor screen at the opposite side of the chamber. This diffraction pattern is a reciprocal space representation of the surface lattice structure. If the surface is atomically smooth (the electron beam samples only the top couple of monolayers of the crystal) a streaky, 2-D diffraction pattern is formed. If the surface is rough a spotty, 3-D diffraction pattern results. The RHEED diffraction pattern thus monitors the quality of the crystal surface.

A.4.2 RHEED Oscillations

As explained in A.3.3, MBE crystal growth proceeds through island growth. When one half of the surface is covered with islands, the surface is maximally rough. The RHEED electron beam is more broadly diffracted by this surface than by the atomically smooth surface present at the completion of a monolayer. Thus the intensity of the RHEED diffraction pattern is modulated as growth proceeds due to the periodic variation in surface roughness. In particular, the intensity of the specular diffraction spot (that is, the direct reflection of the beam) is seen to oscillate, reaching a maximum at the completion of each monolayer. By tracking the intensity of the RHEED pattern, the growth of the crystal can be monitored precisely.

Appendix B

Laser Diode Theory

Any laser consists of a gain medium, a wave guiding structure, and a set of partially reflecting mirrors for optical feedback. In the case of semiconductor laser diodes, gain is produced by electrically pumping a specially designed heterostructure. Wave guidance transverse to the plane of the device is achieved by a slab dielectric waveguide incorporated into the heterostructure. In the device plane, a guiding structure is fashioned lithographically. Optical feedback is produced by using the inherent crystallographic cleave planes to form facets.

This appendix presents a basic explanation of laser operation. Using the device structure of Chapter 7, a simple model of the laser diode is developed. This treatment is far from adequate for a complete understanding of laser physics, but rather puts in context the specific applications of this theory in the present work. For a formal development of this material reference should be made to [88,89,90,91,92,93].

B.1 Basic Laser Operation

Consider an optical cavity formed by a wave guiding medium sandwiched between two partially reflecting mirrors, with field reflection coefficients R_1 and R_2, as in Figure B.1. The medium has optical power loss α_{int}, but a portion of the medium is externally pumped to produce optical power gain, g. This gain medium consists of a two level quantum mechanical system. External pumping increases the occupancy of the upper level. Carriers in this level relax to the lower level, releasing a photon, by either spontaneous or stimulated emission. Carriers in the lower level may be excited to the upper level through the process of absorption. Optical gain is produced when stimulated emission exceeds absorp-

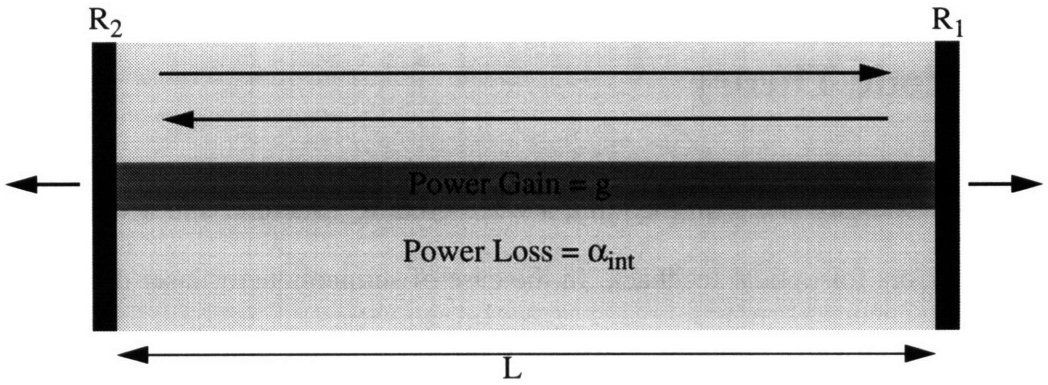


Figure B.1: A prototypical laser. An optical cavity is formed by two partially reflecting mirrors, with field reflection coefficients R_1 and R_2, sandwiching a medium with power loss α_{int}. A portion of the medium is externally pumped to produce optical power gain g. A standing wave is produced by the superposition of backward and forward propagation waves.

tion.

Consider an optical mode propagating in the guiding structure between the mirrors. The complex valued wave number for the traveling wave is

$$k = \kappa - in_{eff}k_0 \tag{B.1}$$

where n_{eff} is the effective index of refraction of the wave guide and $k_0=2\pi/\lambda$ with λ the free space wavelength. The real part of the wave number, κ, produces the exponential rise or fall of the optical field intensity due to loss or gain in the medium. It is given by

$$\kappa = \frac{\Gamma g - \alpha_{int}}{2} \tag{B.2}$$

The factor of 2 converts power gain/loss to field gain/loss. The optical confinement factor, Γ, accounts for the fact that only a fraction of the field interacts with the gain region.

As an optical wave front makes a round trip through the cavity, its amplitude and phase are modified by two passes through the medium and reflection from each mirror. The phasor describing the field is modified by the factor

$$R_1 e^{\kappa L} R_2 e^{\kappa L} = R_1 R_2 e^{(\Gamma g - \alpha_{int})L} e^{-i2n_{eff}k_0 L} \tag{B.3}$$

To obtain a self-consistent solution, the wave front must return to its original phase and amplitude upon completion of a round trip. This means that the factor in (B.3) must equal one. Thus we have

$$R_1 R_2 e^{(\Gamma g - \alpha_{int})L} = 1 \tag{B.4}$$

$$2n_{eff}k_0 L = m2\pi \tag{B.5}$$

where m is an integer.

Substituting k_0 in (B.5) gives

$$\lambda = \frac{2n_{eff}L}{m} \tag{B.6}$$

which establishes what wavelengths of light may exist in the cavity. The laser can only operate at one of these allowed wavelengths. For a typical in-plane laser diode the cavity length, L, is much greater that λ, so the wavelength spacing is fairly small.

Solving for g in (B.4) gives the threshold gain, g_{th}

$$g_{th} = \frac{1}{\Gamma}\left(\alpha_{int} + \frac{1}{L}\ln\left(\frac{1}{R_1 R_2}\right)\right) \tag{B.7}$$

As light bounces back and forth between the mirrors it suffers loss due to absorbtion in the medium and due to extraction through the mirrors. Suppose external pumping is small so that g is less than the total loss. In this case, the field exponentially diminishes to zero. The power being pumped in is primarily spent in spontaneous emission.

By increasing the external pumping, g is increased. At the point where g exactly balances the total loss, spontaneously emitted light is able to make complete round trips without decay. As it does so, it produces stimulated emission of the same phase. A stable state is reached in which all light that is absorbed in the material or extracted from the mirrors is balanced by stimulated emission. With $g=g_{th}$, the laser is at its threshold. Any additional

increase in pumping beyond this point does not produce greater gain, but rather allows the generation more light through stimulated emission. If g was to be larger than the total loss, the field would grow without bound, which is not possible in steady state. The mechanism by which g is clamped is as follows: since the stimulated emission rate increases with field intensity and field intensity increases with stimulated emission rate, a positive feedback loop is formed, but the stimulated emission rate is limited by the external pumping rate, so the increase in field intensity is clamped and stable operation is observed. The stimulated emission rate for the lasing modes increase drastically, while the emission rate into the other modes remains small in comparison. All carriers now recombine into the waveguide/ cavity mode(s) that satisfy the lasing condition. By designing the waveguide to support a single propagating mode, all radiative recombination may be efficiently coupled into a well-directed output beam. It is this phenomenon that gives lasers their great above threshold efficiency.

In summary, externally applied pumping initially increases the gain and produces spontaneous emission. Once $g=g_{th}$, gain exactly balances the total loss in the cavity and is clamped at this value. Beyond this point additional pumping is transferred to coherent light output from the laser.

B.2 Broad Area Laser Diodes

A broad area laser is one in which the optical cavity is formed from a planar, 2-D waveguide structure. This is accomplished by patterning a wide (~100 μm) ohmic contact on top of the laser heterostructure (to be described next). The wafer is lapped to reduce series resistance and ease facet cleaving, and a back side ohmic contact is applied. Finally facets are formed by cleaving the sample perpendicular to the stripes. A broad area laser diode based on the InGaAs/GaAs/InGaP QW-SCH used in this thesis is schematically shown in Figure B.2.

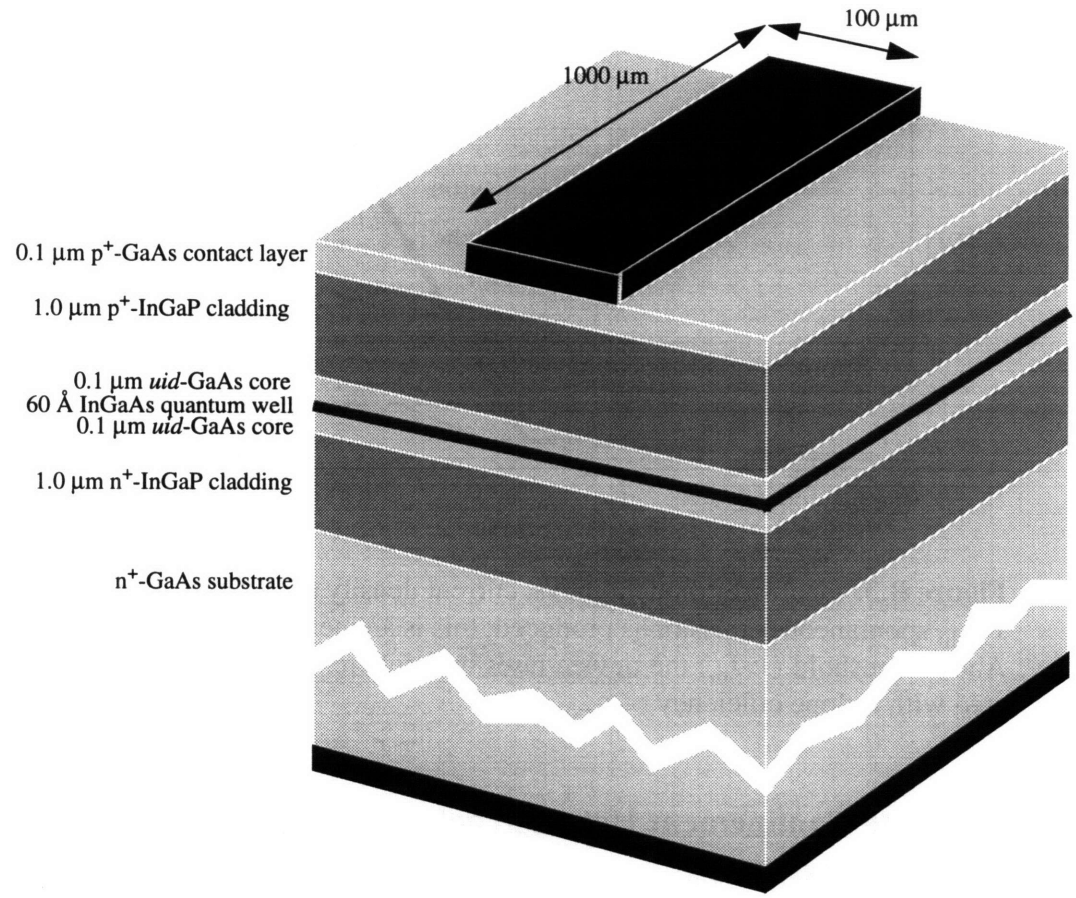


Figure B.2: Broad area laser diode based on InGaAs/GaAs/InGaP quantum well separate confinement heterostructure (QW-SCH). Following growth of the device structure, a broad ohmic contact stripe is photolithographically patterned. The substrate is thinned by lapping and a back side ohmic contact is made.

Typical cavity lengths are several hundred microns to over one millimeter. By making the cavity very long (~1 mm) the loss from the end facets become insignificant compared to material losses. The broad area laser is thus important because it allows accurate comparison of laser heterostructures and material quality.

Static laser operation is summarized in a plot of the light output versus the current density input. This is referred to as an L-I curve. An example is given in Figure B.3. The ideal laser, under static operation, is thus characterized by its threshold current density, J_{th}, and its above threshold external efficiency, η_{ext}.

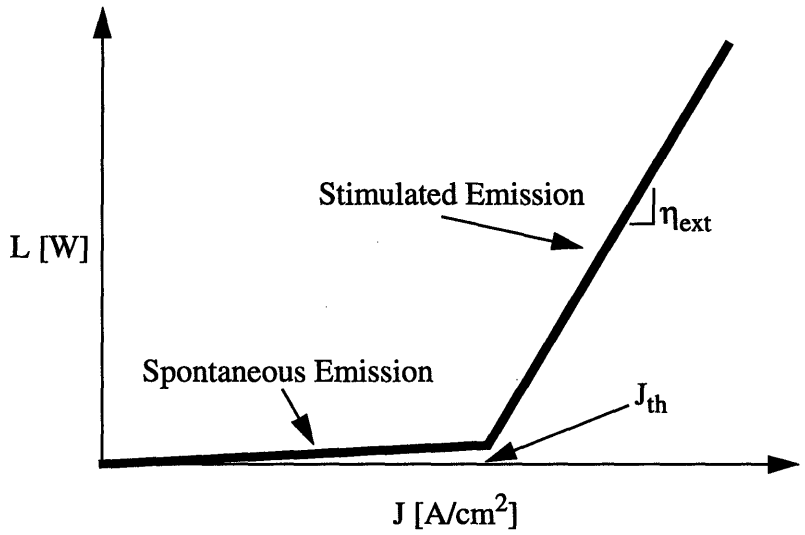


Figure B.3: Ideal laser diode light vs. current density (L-I) curve. For $J<J_{th}$, spontaneous emission is produced; this is an inefficient process. Above threshold ($J>J_{th}$) the device lases and coherent light is generated with a slope efficiency of η_{ext}.

B.3 The Separate Confinement Heterostructure

As discussed above, a laser is composed of a waveguide structure, a gain medium, and partially reflecting mirrors for optical feedback. To fabricate semiconductor lasers, the mirrors are formed by using the inherent cleave planes of the crystal to form very smooth facets. In-plane waveguiding is normally achieved by fabricating a type of stripe waveguide.

The semiconductor heterostructure serves two purposes: confinement of an optical mode and generation of optical gain (which requires the confinement of electrical carriers in the active region). In this section, the basic quantum well separate confinement heterostructure (QW-SCH) is described. As seen in Figure 7.1 and Figure B.2 for the case of InGaP based lasers, the QW-SCH consist of a quantum well (InGaAs) at the center of a core region (GaAs), which is in turn surrounded by wide cladding regions (InGaP). The term "separate confinement" refers to the fact that the optical field and the electrical carri-

ers are confined by different layers. Various other important design modifications, presented in Section 2.4, allow optimization of the optical mode profile and carrier injection efficiency. Figure B.4 summarizes both the optical mode confinement and current generation features of the QW-SCH.

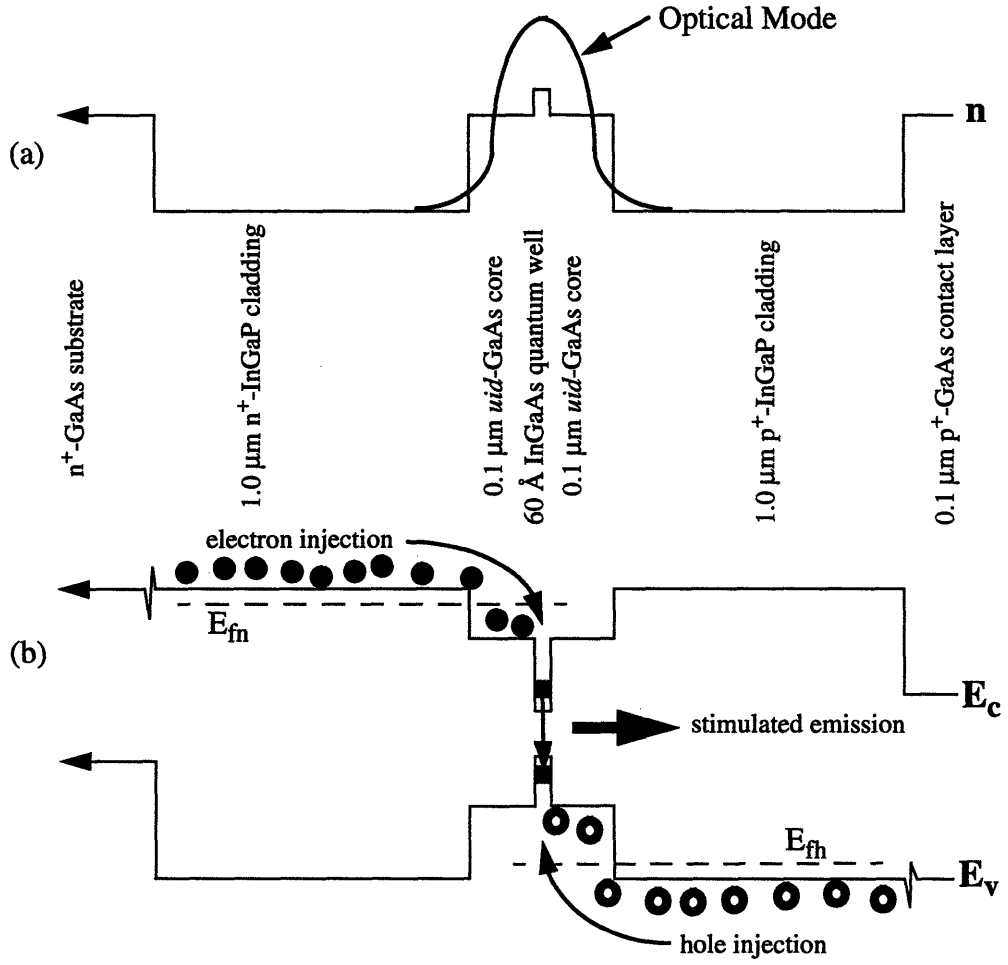


Figure B.4: Optical and electrical operation of QW-SCH. The variation of the material index of refraction, *n*, throughout the SCH is shown in (a). The high refractive index GaAs core and low index InGaP claddings form a dielectric slab waveguide to confine the optical mode. (b) shows the conduction and valence band profiles. The quantum well confines injected carriers where they recombine by stimulated emission.

B.3.1 Optical Confinement

A dielectric slab waveguide is formed by the high refractive index GaAs core and the low index InGaP claddings. Normally, a GaAs contact layer on top eases ohmic contact formation and the structure sits on a GaAs substrate. Rigorously, this makes the waveguide lossy, but the field falls off exponentially in the cladding layers and has little interaction with these outer GaAs layers. Also, the presence of the quantum well is a very small perturbation on the waveguide. Thus the analytical solution to the three layer case is a very good approximation to the mode profile within the QW-SCH.

In-plane semiconductor lasers emit in the transverse electric (TE) mode. This mode is favored because the facets reflect TE radiation more efficiently than TM radiation. Furthermore, in quantum well devices, only the TE mode produces stimulated emission due to the selection rule for the recombination process. For wave propagation in a symmetric three layer waveguide, the electric field profile is a peaked sinusoid at the center of the core and exponentially decays in the claddings, as depicted in Figure B.4. The optical confinement factor, Γ, is the ratio of the integral of $|E|^2$ over the quantum well with respect to the integral over the entire structure. In determining gain, it is $|E|^2$ that drives the stimulated emission process. Thus the Γ ratio accounts for what fraction of the field actually interacts with the gain medium.

B.3.2 Electrical Confinement

The electrical carriers are confined in the quantum well where they recombine radiatively by stimulated emission. Under high injection, as is usually the case, the bands are essentially flat [94]. Electrons and holes are transported through the heavily doped n- and p-type claddings by drift. They are injected into the intrinsic GaAs region where they dif-

fuse into the quantum well and, ideally, are captured and radiatively recombine. Excess carriers present a large deviation from thermal equilibrium only in the intrinsic core and active regions. Since recombination processes act to return a system to equilibrium, the material quality in regions containing large numbers of minority carriers is very important to device performance. These regions include the undoped core and quantum well regions and the interfaces between the core and claddings.

B.3.3 Gain

In a two level system, electron-photon interactions proceed through three processes: stimulated emission, absorption, and spontaneous emission. Transition rates are given in terms of the Einstein A and B coefficients [88], which must be calculated quantum mechanically using Fermi's Golden rule with the electromagnetic interaction Hamiltonian [93]. The probability of stimulated emission and absorption are determined by identical B coefficients and are proportional to the square of the electric field magnitude, $|E|^2$. The probability of spontaneous emission is determined by the A coefficient, which is proportional to the B coefficient. All rates depend on the availability of initial and final states. Since absorbtion and stimulated emission depend on the same constant, the only way to achieve gain is to maintain "population inversion", that is, to have more carriers in the upper level. In the case of semiconductor lasers where the two levels are actually the conduction and valence bands, the Bernard-Duraffourg condition specifies the transparency point, at which gain equals material loss. This condition states that the difference in the quasi-Fermi levels must exceed the energy of the transition.

Due to the proportionality between the A and B coefficients, gain is proportional to the spontaneous recombination rate, R_{sp}. In turn, R_{sp} is approximately proportional to n/t_{sp}.

So, gain is proportional to carrier concentration n. And since n is proportional to the injected current density, we have

$$g = \frac{\beta \eta_{int} (J - J_{tr})}{d} \tag{B.8}$$

where d is the thickness of the quantum well, J_{tr} is the "transparency" current density at which the Bernard-Duraffourg condition is met, β is the linear differential gain coefficient, and η_{int} is the "internal quantum efficiency". η_{int} represents the fraction of electrons injected at the terminals that are converted to photons by stimulated emission, and is a function of the heterostructure and material quality.

B.3.4 Threshold Current Density, J_{th}

By combining (B.7) and (B.8), the threshold current density can be written as

$$J_{th} = J_{tr} + \frac{d}{\eta_{int} \Gamma \beta} \left(\alpha_{int} + \frac{1}{L} \ln \left(\frac{1}{R_1 R_2} \right) \right) \tag{B.9}$$

Thus, J_{th} depends on the heterostructure design and material quality through η_{int} and α_{int}. R_1 and R_2 are nominally 1/3 for III-V semiconductor to air interfaces. Γ, d, and L are design parameters, and β depends on the choice of quantum well structure.

B.3.5 External Efficiency, η_{ext}

As defined above, η_{int} converts terminal current to photon generation rate. The optical power emitted from the quantum well is thus

$$L_{int} = A (J - J_{th}) \frac{\eta h \nu}{q} \tag{B.10}$$

where A is the active region area. To convert to output power, the photon extraction efficiency must be factored in. This is the ratio of photons lost through the facets to the total loss of photons. Thus

$$L = L_{int}\frac{\frac{1}{2L}\ln\left(\frac{1}{R_1R_2}\right)}{\alpha_{int}+\frac{1}{2L}\ln\left(\frac{1}{R_1R_2}\right)} \tag{B.11}$$

The external efficiency is defined as the fraction of electrons injected at the terminal that are extracted. It can be determined experimentally from the L-I curve using

$$\eta_{ext} = \frac{d\left(\frac{L}{h\nu}\right)}{d\left(\frac{A}{q}(J-J_{th})\right)} \tag{B.12}$$

Analytically this reduces to

$$\frac{1}{\eta_{ext}} = \frac{1}{\eta_{int}}\left(1+\frac{\alpha_{int}}{\ln\left(\frac{1}{R}\right)}L\right) \tag{B.13}$$

where it has been assumed that R_1=R_2=R.

Appendix C

Device Characterization

C.1 LED Characterization

Figure C.1 is a sketch of the setup used to characterize the electrical and optical characteristics of the broad area LED structures and fully processed and integrated AlGaAs based LEDs discussed in Chapter 6. A computer collects data from an HP 4145 parameter ana-

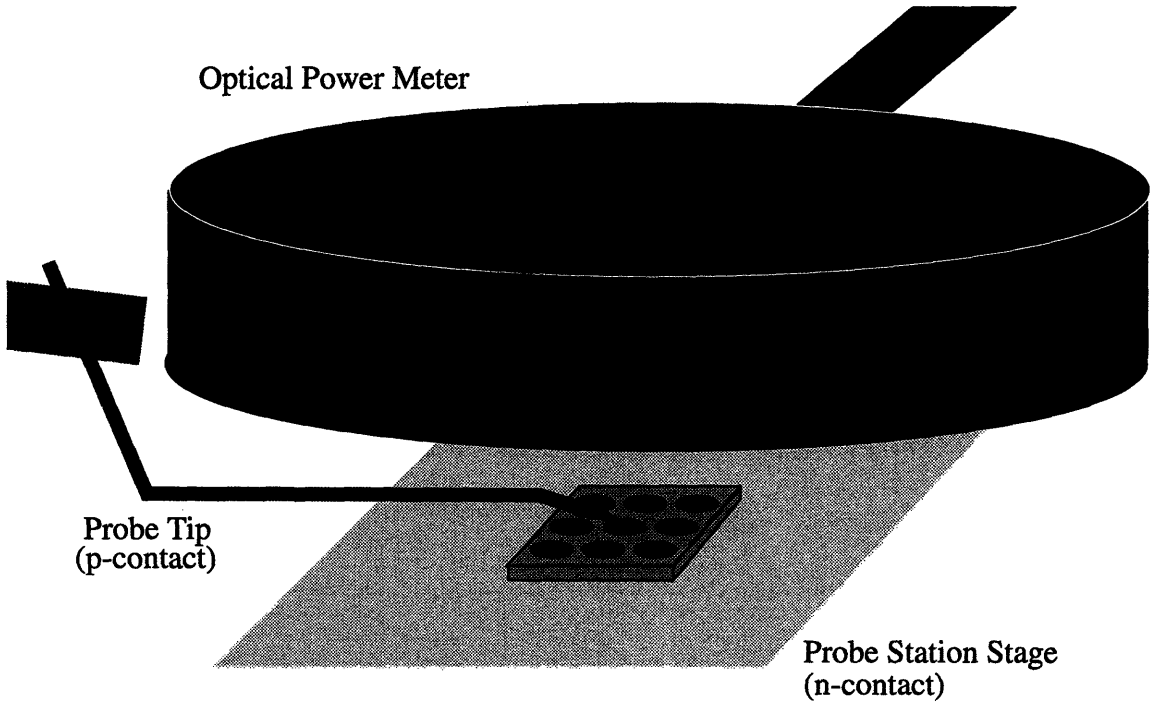


Figure C.1: Measurement setup for broad area LED characterization. The sample, with back side ohmic metal, sits on the probe station stage, which makes the n-side contact to the diode. The surface of the sample is metallized with 500 μm diameter spots which are probed by a specially angled probe tip. The head of an optical power meter is place around 4 mm from the sample. An HP 4145 parameter analyzer, connected to a computer, controls the voltage applied and monitors the current between the probe tip and stage. The output of the power meter is also controlled by the HP 4145.

lyzer. The HP 4145 controls the voltage applied between the probe that is placed on the device's p-type contact and the probe station's stage. The current through the device is

monitored to yield the diode's current-voltage characteristics. To monitor the optical output, a Coherent model 212 power meter is placed approximately 4 mm from the sample. The active area of the detector is 7 mm in diameter and is set back around 7 mm into the head of the detector.

C.2 Pulsed Laser Characterization

Pulsed room temperature characterization of the broad area laser diodes discussed in Chapter 7 used 1 μs pulses at a 1 KHz repetition rate yielding a duty cycle of 0.1%. The pulses were generated by an Avtec pulse generator triggered by a frequency generator. The pulse amplitude was set by a computer. The pulses are applied across the diode, as sketched in Figure C.2, through a diode protection/current monitor circuit. This circuit is

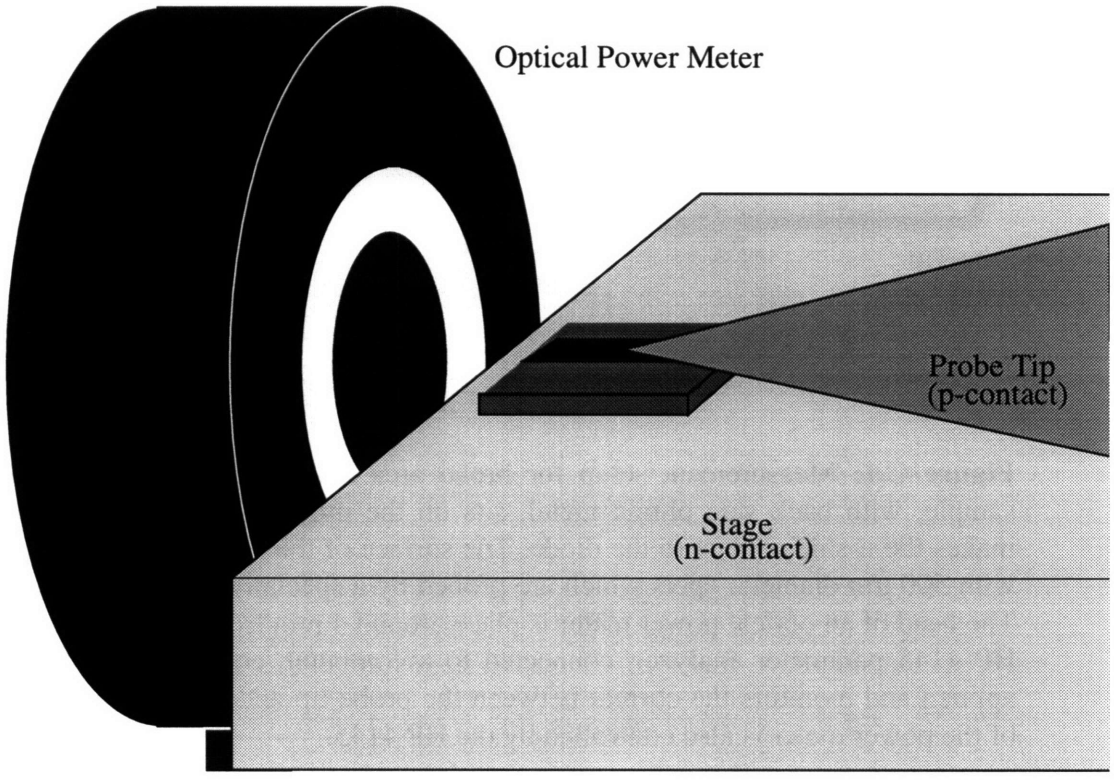


Figure C.2: Pulsed broad area laser test setup. A broad probe tip contacts the stripe (diode p-contact) of the laser. The n-type connection is made through the stage. A power meter is used to collect the emission.

diagrammed in Figure C.3. A reverse biased diode prevents the Avtec from applying a

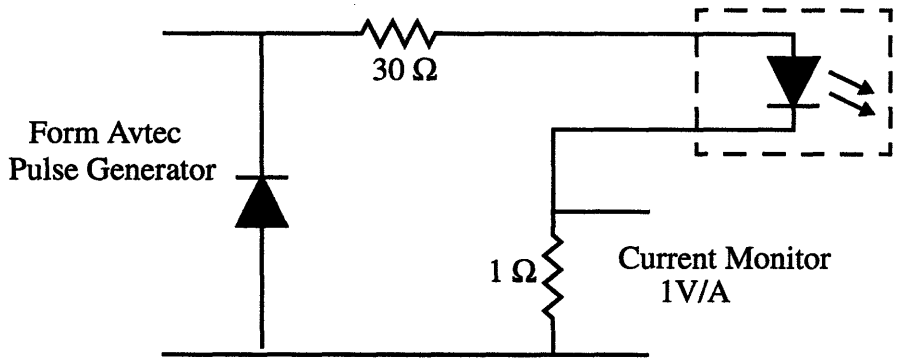


Figure C.3: Circuit used to protect laser diode from reverse bias and to monitor its terminal current.

negative bias across the laser. A 30 Ω resistor is used to damp out ringing, and a 1 Ω resistor is used to monitor the current. The voltage across this resistor and the output of a Coherent model 212 power meter, placed in front of the laser, are fed into a boxcar integrator which samples them in synch with the trigger pulses and averages over many samples to reduce noise. The DC value generated by the boxcar integrator is then digitized and read into the computer.

Calculation of internal quantum efficiency of broad area lasers characterized by this setup were found to be inconsistent with measured threshold current densities. The discrepancy indicates that the optical power is being underestimated by a factor of 2 to 3.

Appendix D

Vitesse Semiconductor HGaAs3 E/D MESFET Process

The Vitesse HGaAs3 E/D MESFET process produces self-aligned enhancement and depletion mode metal-semiconductor field effect transistors (MESFETs) and multiple levels of electrical interconnects. In addition, Schottky barrier diodes and metal-semiconductor-metal (MSM) photodetectors may be created using the standard gate metallization.

The thirty-eight step, thirteen mask process flow is briefly described here, following the Vitesse Foundry Design Guide [95]. The tables and figure are taken from Braun, *et. al.*, [17]. The process uses four inch undoped GaAs substrates. Table D.1 lists the steps, which are diagrammed (up to the first layer of metallization) in Figure D.1, and described below.

Step 1, 2: The substrate wafer is cleaned and capped with a field oxide which is patterned to define the device active areas.

Step 3, 4, 5: Silicon is ion implanted to form the MESFET channels. The dose is controlled to produce the correct threshold voltage for enhancement-mode transistors. The active areas of the depletion-mode devices are then lithographically patterned and additional silicon ions are implant to lower the threshold voltage.

Step 6, 7: The tungsten nitride refractory gate metal is deposited by reactively ion sputtering tungsten in a nitrogen ambient. $W_{1-x}N_x$ with x=0.1-0.2 is produced. The gate metal is then patterned using standard lithographic techniques.

Step 8: A light implant, referred to as the LDD implant, is applied to reduce the series resistance from the source and drain to the channel.

Step	Process
1	Field Oxide deposition
2	Mask 1, active area definition
3	Enhancement device implant
4	Mask 2, depletion implant definition
5	Depletion device implant
6	Gate metal deposition
7	Mask 3, gate metal definition
8	LDD implant
9	Spacer oxide deposition
10	Anisotropic spacer etch
11	Source and drain implant
12	Oxide 0 deposition
13	Activation Anneal
14	Mask 4, ohmic contact metallization
15	Ohmic contact sintering
16 (Metal 1)	Oxide 1 deposition
17 (Metal 1)	Mask 5, via 1 definition
18 (Metal 1)	Metal 1 deposition
19 (Metal 1)	Mask 6, Metal 1 definition
20 (Metal 1)	Metal 1 etch
21-25 (Metal 2)	Repeat 16-20 for Metal 2
26-30 (Metal 3)	Repeat 16-20 for Metal 3
31-35 (Metal 4)	Repeat 16-20 for Metal 4
36	Passivation Dielectric deposition
37	Mask 13, passivation contact definition
38	Passivation dielectric etch

Table D.1: Vitesse HGaAs3 Fabrication Sequence [17]

Step 9, 10, 11: A spacer dielectric is deposited and patterned around the gates. A high dose silicon ion implant is used to form the source and drain regions. The spacer dielectric protects the channel region from this implant.

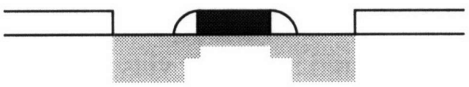
Step 12, 13: Layers of silicon nitride and silicon dioxide are deposited to cap the implant regions. The implants are then activated by annealing for one hour at 800°C.

(1) Field Oxide deposition
(300Å Si_3N_4, 3500Å SiO_2)
(2) Active area definition

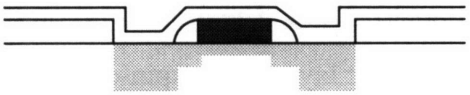
(3) Enhancement device implant (Si)
(4) Depletion implant definition
(5) Depletion device implant (Si)

(6) Gate metal deposition
(3500Å WN_x)
(7) Gate metal definition

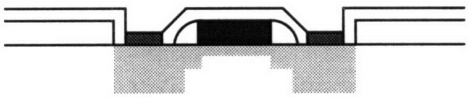
(8) LDD implant (Si)



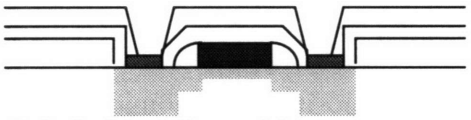
(9) Spacer oxide deposition (SiO_2)
(10) Anisotropic spacer etch
(11) Source and drain implant (Si)



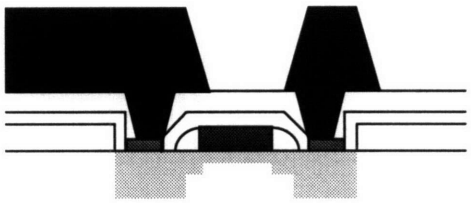
(12) Oxide 0 deposition
(375A Si_3N_4, 1600Å SiO_2)
(13) Activation Anneal (800C, 1 hour)



(14) Ohmic contact metallization
(700Å Ni-Ge, 1000Å WN_x)
(15) Ohmic contact sintering
(550C, 30 minutes)



(16) Oxide 1 Deposition
(3000Å SiO_2)
(17) Via 1 definition



(18) Metal 1 deposition
(1500Å WN_x, 8000Å $AlCu_x$, 1000Å WN_x)
(19) Metal 1 interconnect definition
(20) Metal 1 etch

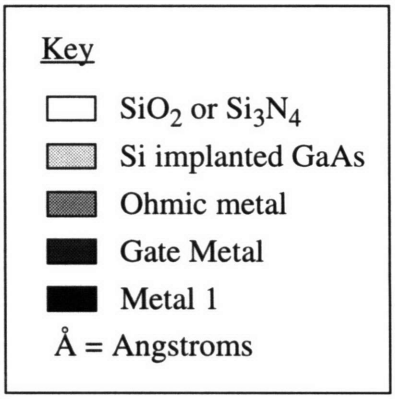


Figure D.1: HGaAs3 Process Flow Schematic through Metal 1 [17]

Step 14, 15: Ohmic contacts are formed from Ni-Ge and capped with a tungsten-nitride barrier layer. The contacts are sintered at 550°C for 30 minutes.

Five steps (two mask layers) are required to form each layer of metal interconnection. The following steps are repeated for each of the four "upper level" metal layers:

Step 16, 17: Silicon dioxide, which forms the intermetal dielectric, is deposited at 380°C. Vias are opened to contact the gate and ohmic metals.

Step 18, 19, 20: The upper level metal consists of an aluminum $Al_{0.99}Cu_{0.01}$ core sandwiched between tungsten-nitride claddings (same material as the gates). The maximum temperature the chips are exposed to in this process is 200°C.

Step 36, 37,38: The process is completed by application and patterning of the passivation dielectric layer. After spin-on-glass (SOG) is hot plate cured at 200°C, vias are etched to the underlying metal 4 layer, exposing the bond pads.

Following steps 1-38, an additional mask step, referred to as the boundary step, is performed to define saw openings in the dielectric stack to allow chips to be cut from the wafer. This step was eliminated in later versions of the process, but can be inserted by special request.

The composition and nominal thickness of each dielectric and metal layer is summarized in Table D.2. For the three metal layer process used in previous designs, the total dielectric/metallization stack thickness was around 3.7 μm. This sets the total thickness of epitaxial material that must be grown in order to attain planarity after the polycrystalline material is removed.

Layer	Composition	Thickness (Angstroms)	Deposition Method	Deposition Time/Temp.
Field oxide	Si_3N_4/SiO_2	200/3500	PECVD	20min/380°C
Oxide 0	Si_3N_4/SiO_2	375/1600	PECVD	10min/380°C
Gate Metal	WN_x	3500	RIS	10min/<100°C
Ohmic Metal	Ni-Ge/WN_x	700/1000	RIS	5min/<100°C
Metal 1	$WN_x/AlCu_x/WN_x$	1500/8000/1000	RIS	10min/<200°C
Oxide 1	SiO_2	3000	PECVD	15min/380°C
Metal 2	$WN_x/AlCu_x/WN_x$	1000/12500/1000	RIS	15min/<200°C
Oxide 2	SiO_2	10000	PECVD	50min/380°C
Metal 3	$WN_x/AlCu_x/WN_x$	1500/17000/1000	RIS	20min/<200°C
Oxide 3	SiO_2	15000	PECVD	75min/380°C
Metal 4	$WN_x/AlCu_x$	1500/17000	RIS	20min/<200°C
Oxide 4	SiO_2	15000	PECVD	75min/380°C
Passivation	SOG	10000	SOG	<1hour/200°C

Table D.2: HGaAs3 Dielectric and Metal Layer Deposition Characteristics [17]

PECVD: Plasma Enhanced Chemical Vapor Deposition
RIS: Reactive Ion Sputtering
SOG: Spin on Glass

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